

AMD BRAZOS

Muxless Discrete/UMA Schematics Document

AMD Ontario CPU FT1

AMD GPU Seymour XT S3

2010-12-01

REV : SA

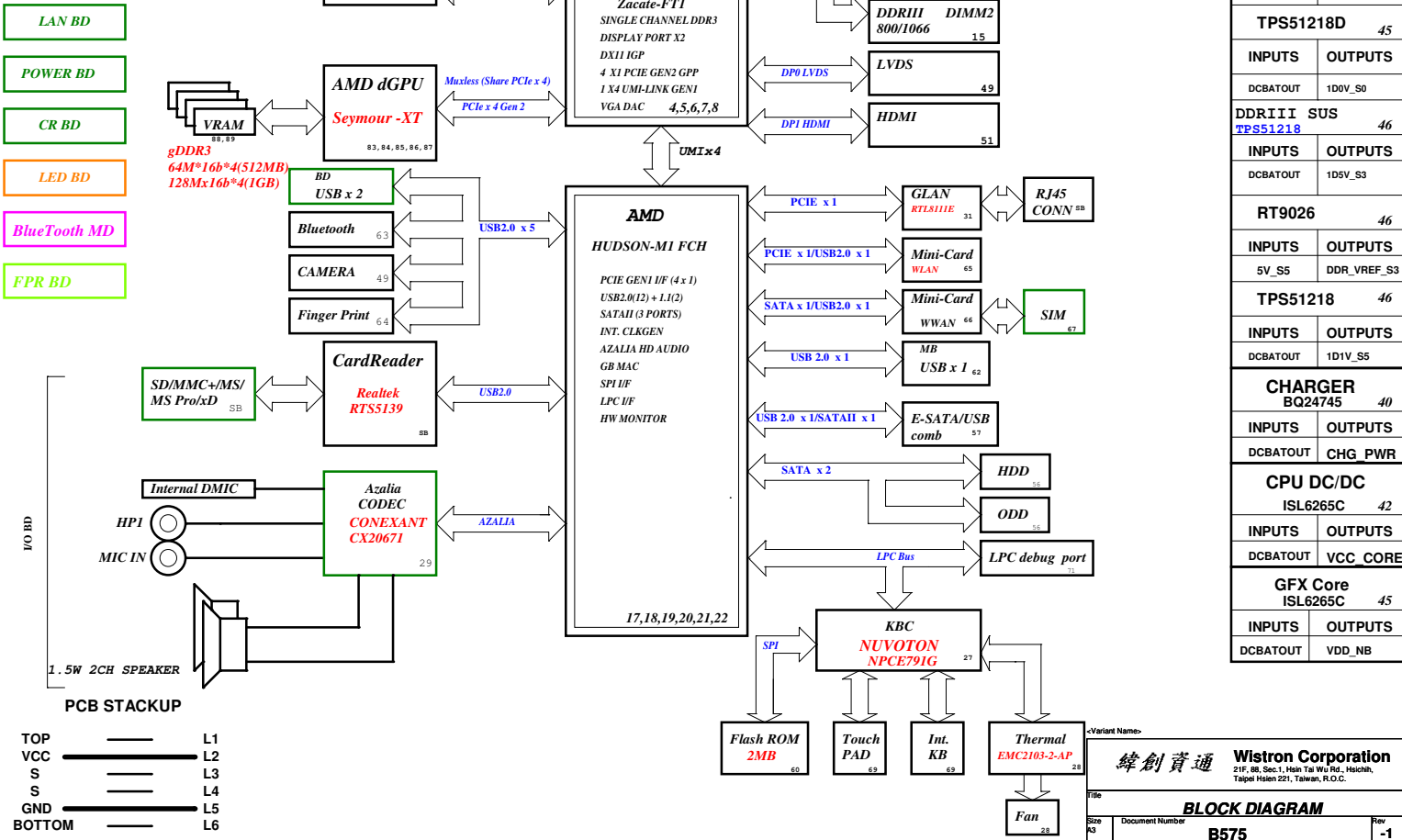
DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX
ROB:ROBSON

<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.			
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Cover Page			
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PROJECT CODE : 91.4PN01.001
PCB P/N : 10332
REVISION : SA

Block Diagram



VGA	
RT8208B	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_FWR
AMD GPU CORE	
TPS51218D	47
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

SYSTEM DC/DC	
TPS51123	41
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 5V_AUX_S5 3D3V_AUX_S5

TPS51218D	
45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

DDR3 III SUS	
TPS51218	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

RT9026	
46	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3

TPS51218	
46	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

CHARGER	
BQ24745	40
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR

CPU DC/DC	
ISL6265C	42
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX Core	
ISL6265C	45
INPUTS	OUTPUTS
DCBATOUT	VDD_NB

PCB STACKUP	
TOP	L1
VCC	L2
S	L3
S	L4
GND	L5
BOTTOM	L6

緯創資通

Wistron Corporation

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Size

Document Number

Date

Block Diagram

B575

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-1

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REQUIRED SYSTEM STRAPS ?

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

USB Table

Pair	Device
0	Internal #3 (MB)
1	WLAN/WIMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1 (IO BD)
6	External #2 (IO BD)
7	CAMERA (HS)
8	Finger Print
9	CardReader
10	NC
11	NC
12	NC
13	NC

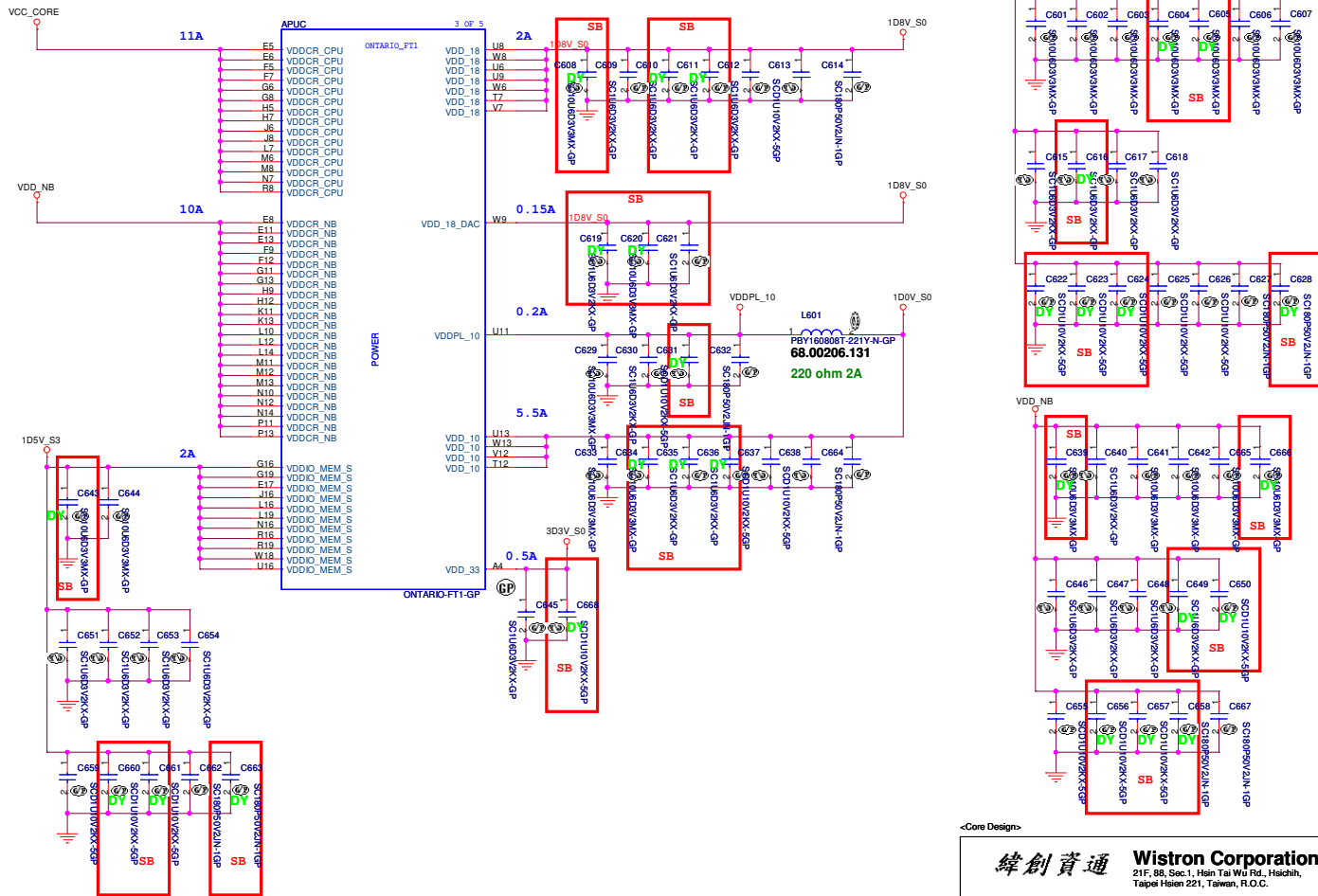
PCIe Routing

	APU
LANE0	PEG
LANE1	
LANE2	
LANE3	
	FCH
LANE0	LAN
LANE1	WWAN
LANE2	WLAN
LANE3	CardReader

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

<Variant Name>		緯創資通 Wistron Corporation	
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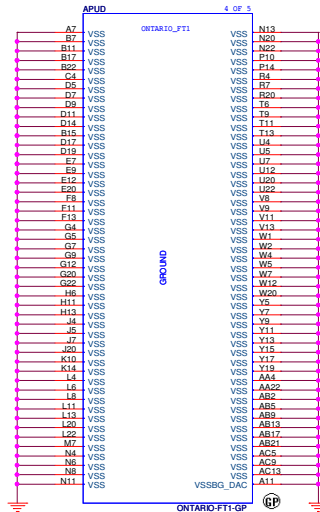


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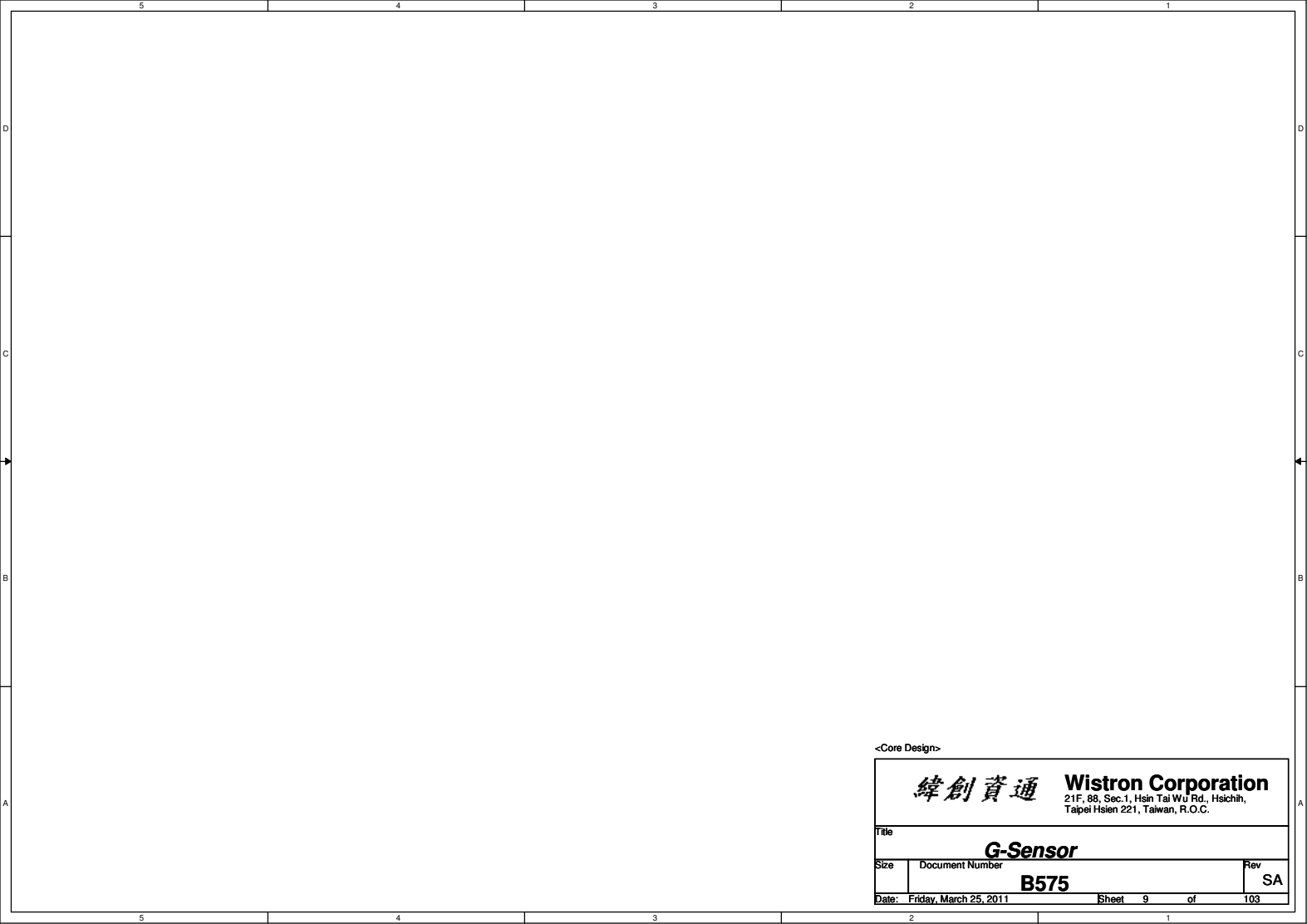


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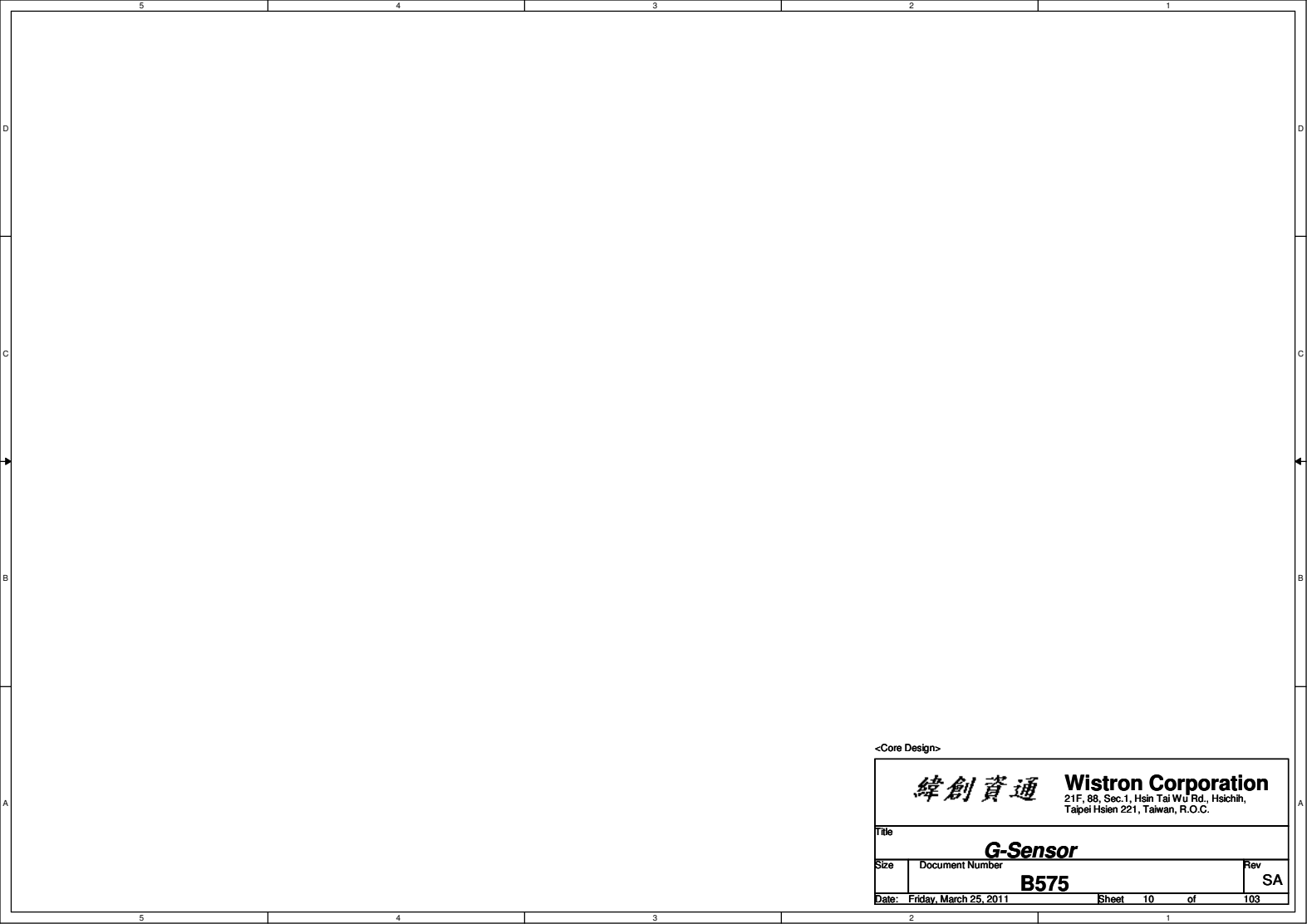
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 321, Taiwan, R.O.C.

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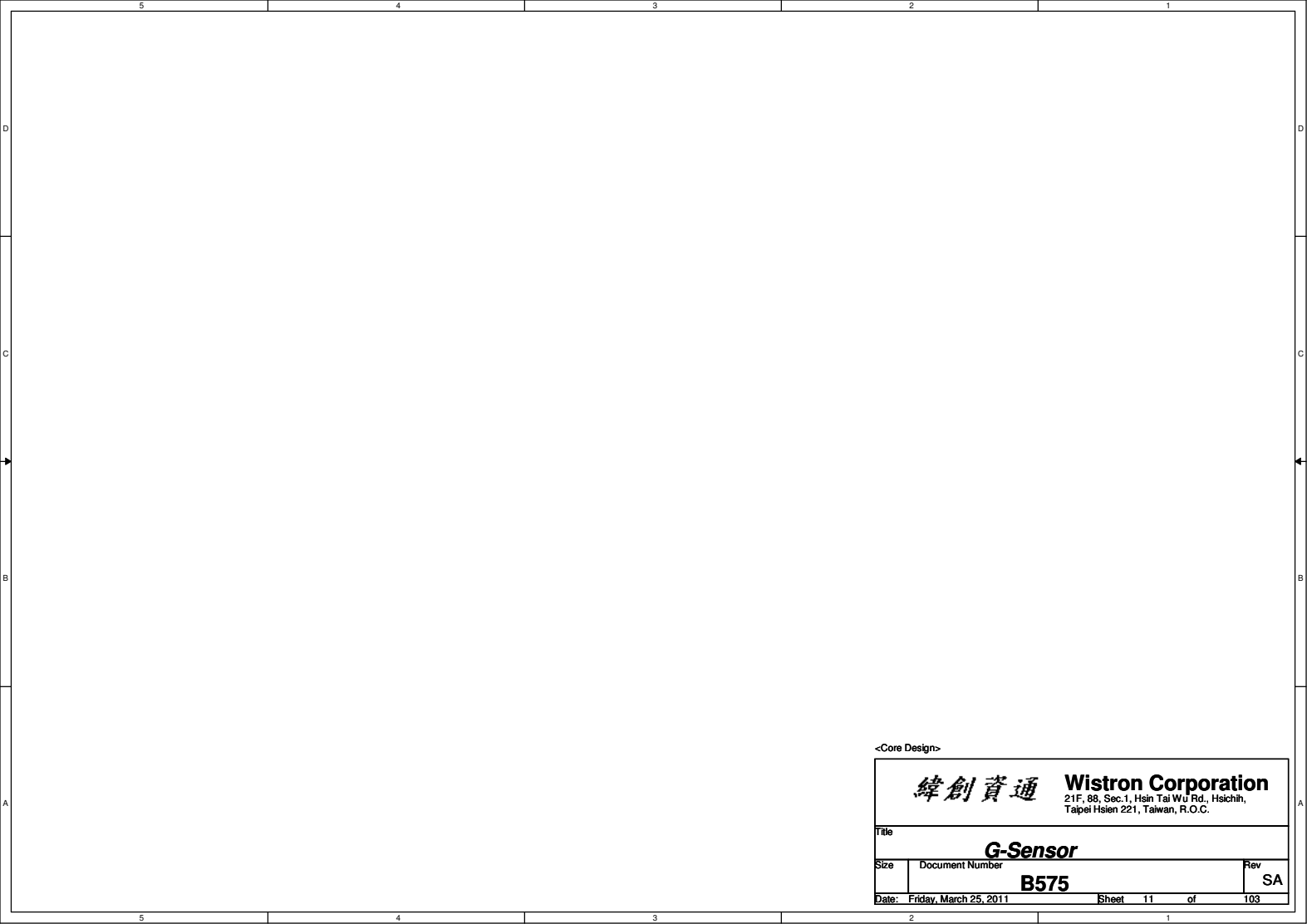
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G-Sensor			
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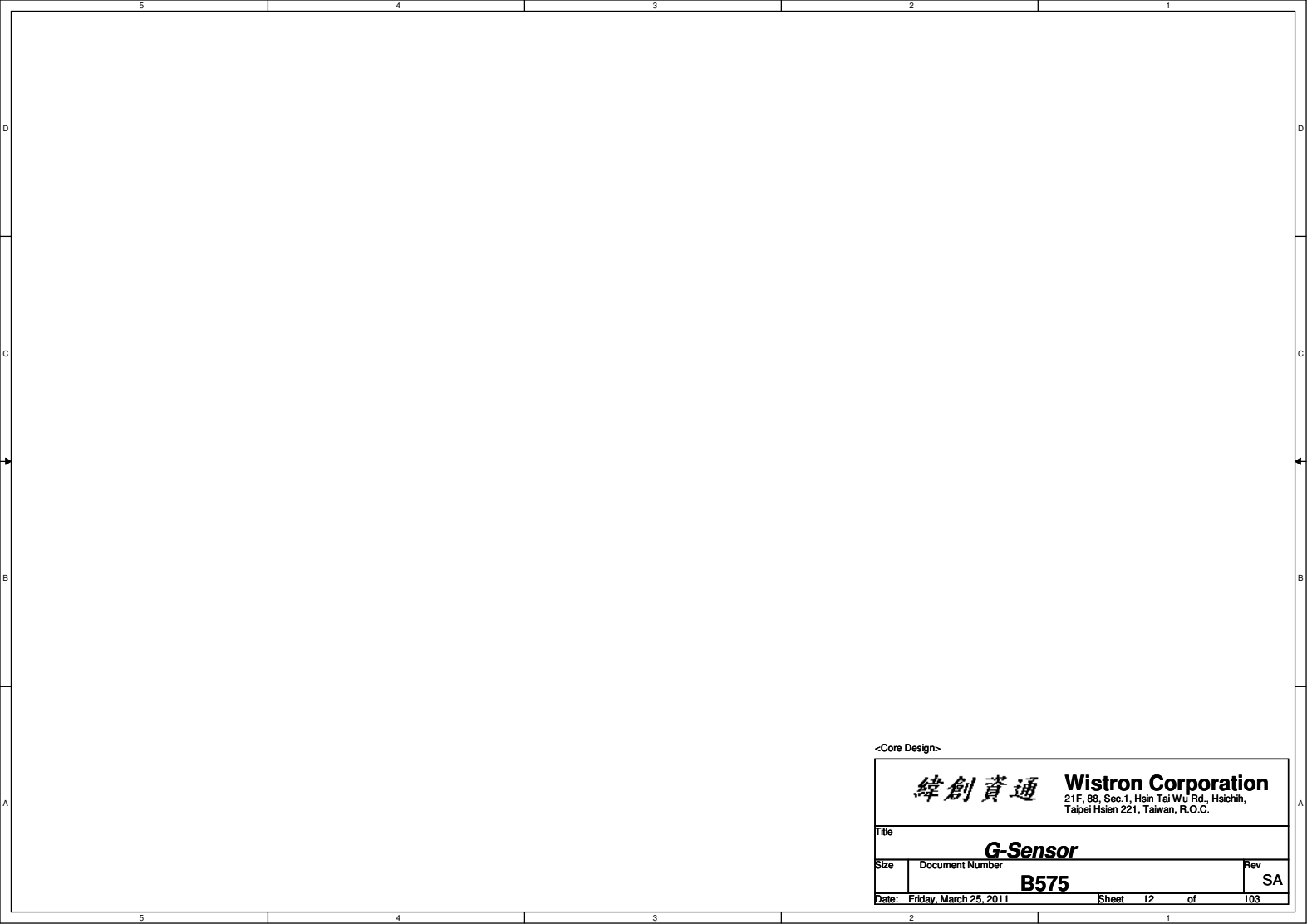
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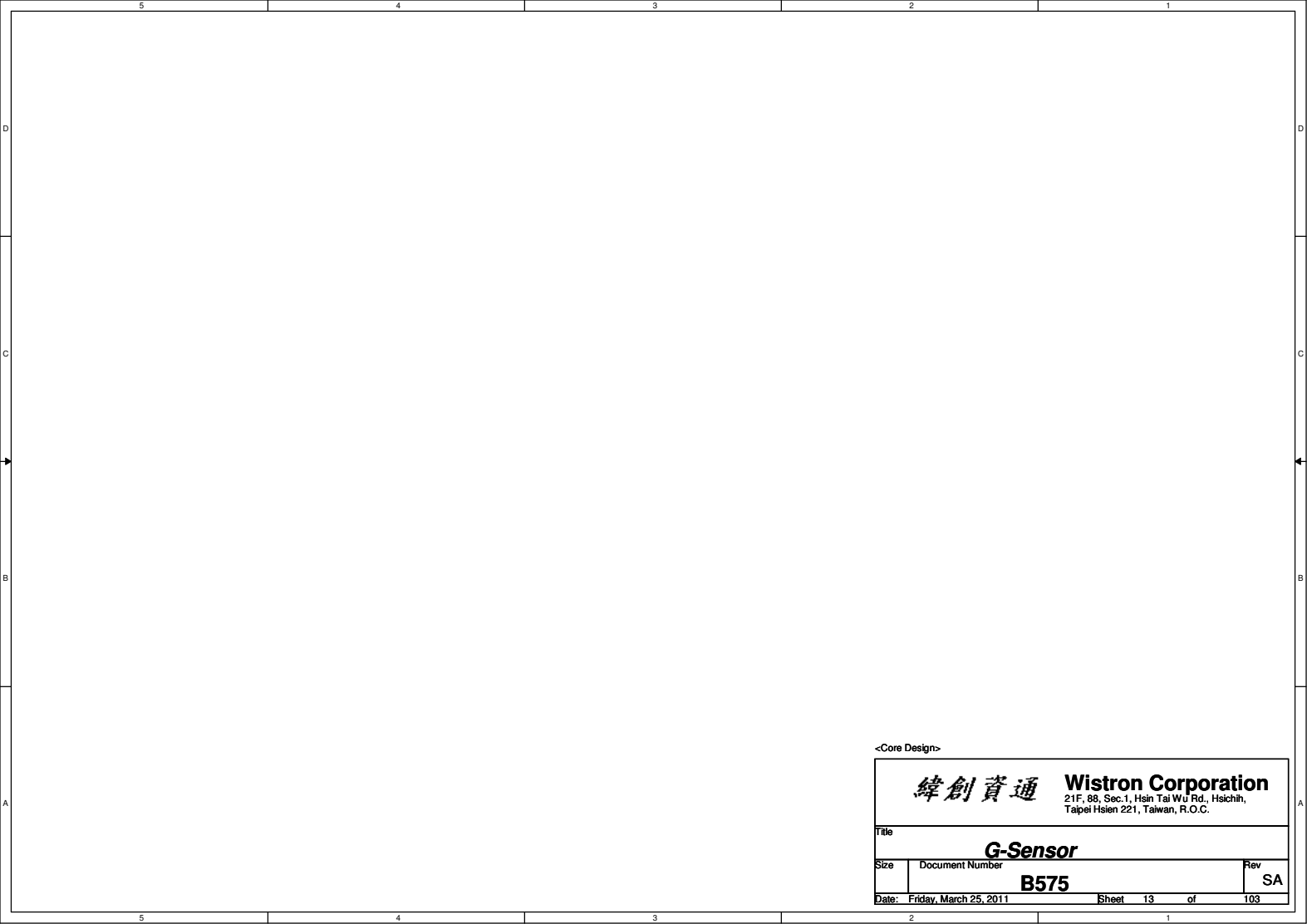
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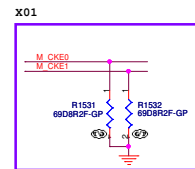
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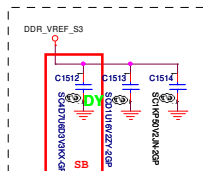


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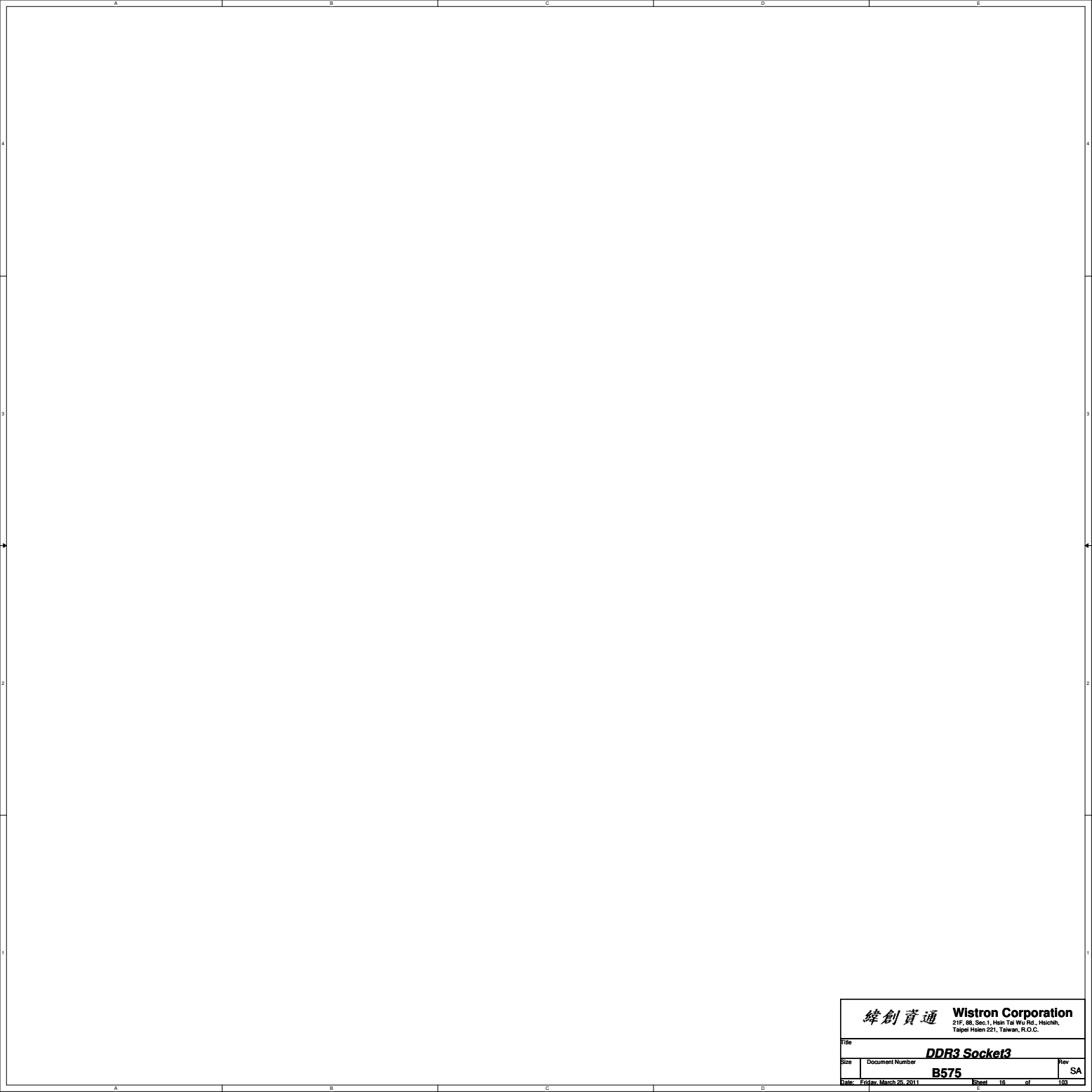
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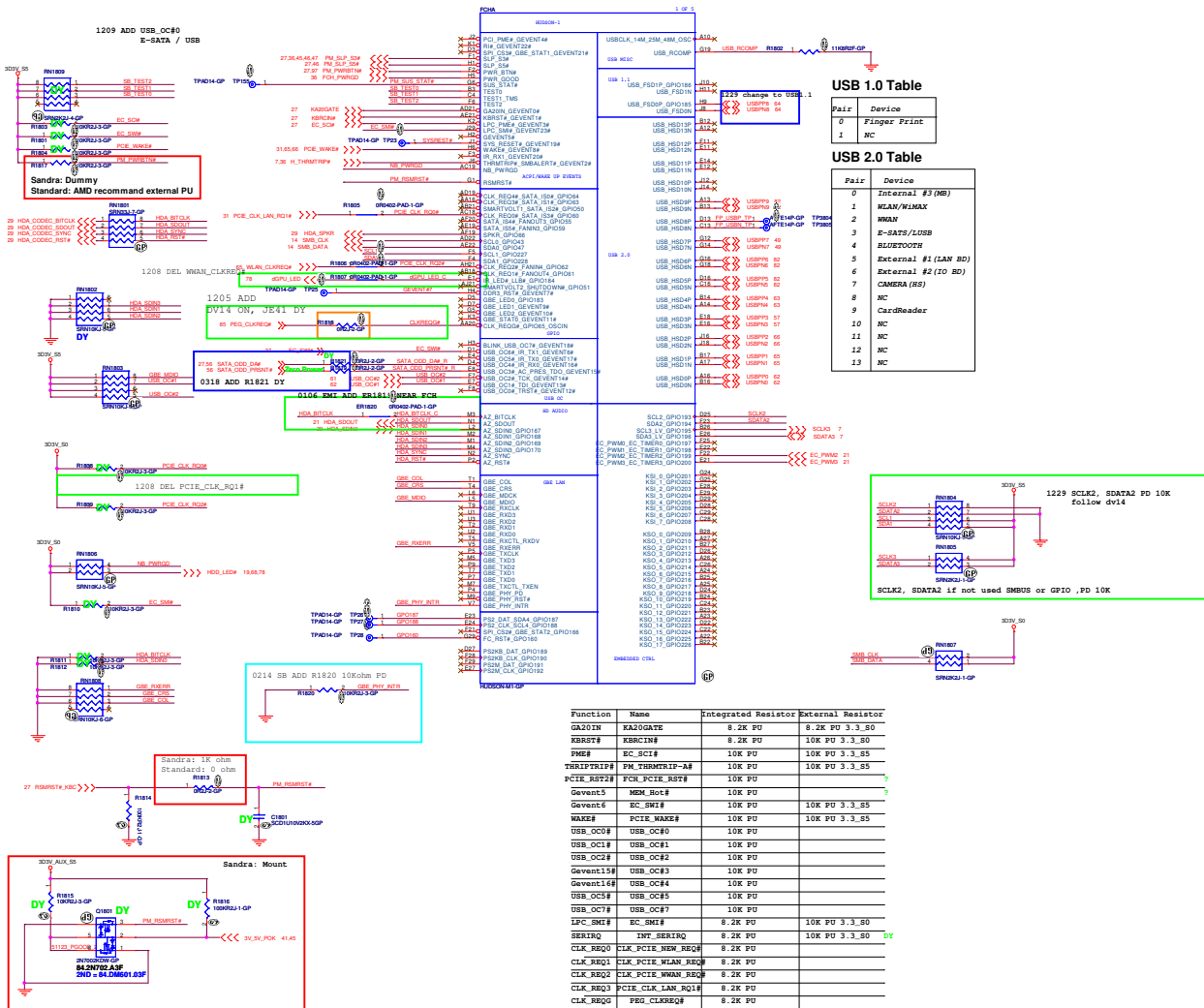
Intel HR DM tied to GND
AMD still following previous design



Place these caps close to VTT1 and VTT2.



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DDR3 Socket3				
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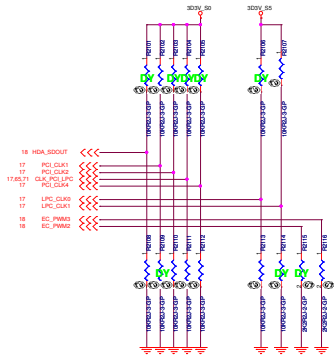
DVT 1ST



SSID = S.B

REQUIRED STRAPS

CBB-PU 3.3V_AUX_85
checklist:PU 3.3V_85
confirm by AMD, following CBB suggestion



REQUIRED SYSTEM STRAPS

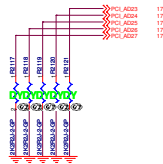
	AZ_SSDOUT (AZC_SSDATAOUT_1)	PCI_CLK1	PCI_CLK2	PCI_CLK3 (CLK_PCI_LPC)	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	Low Power Mode	Allow PCE GEN2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC (Use Internal)	CLKGEN ENABLED (Use Internal)
PULL LOW	Performance Mode DEFAULT	Force PCE GEN1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USE this pin to determine INT/EXT CLK

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPIROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

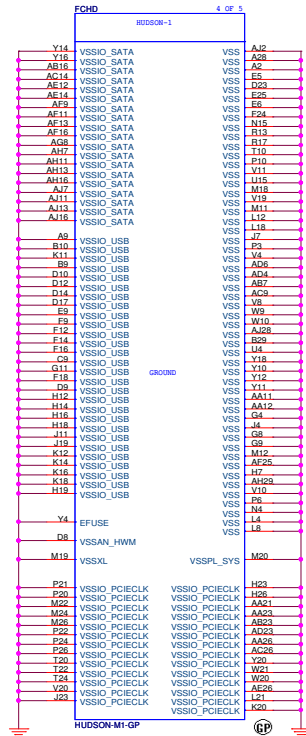
DEBUG STRAPS



	PCI_AD27	PCI_AD28	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT POE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM POE STRAPS	Enable PCI MEM BOOT

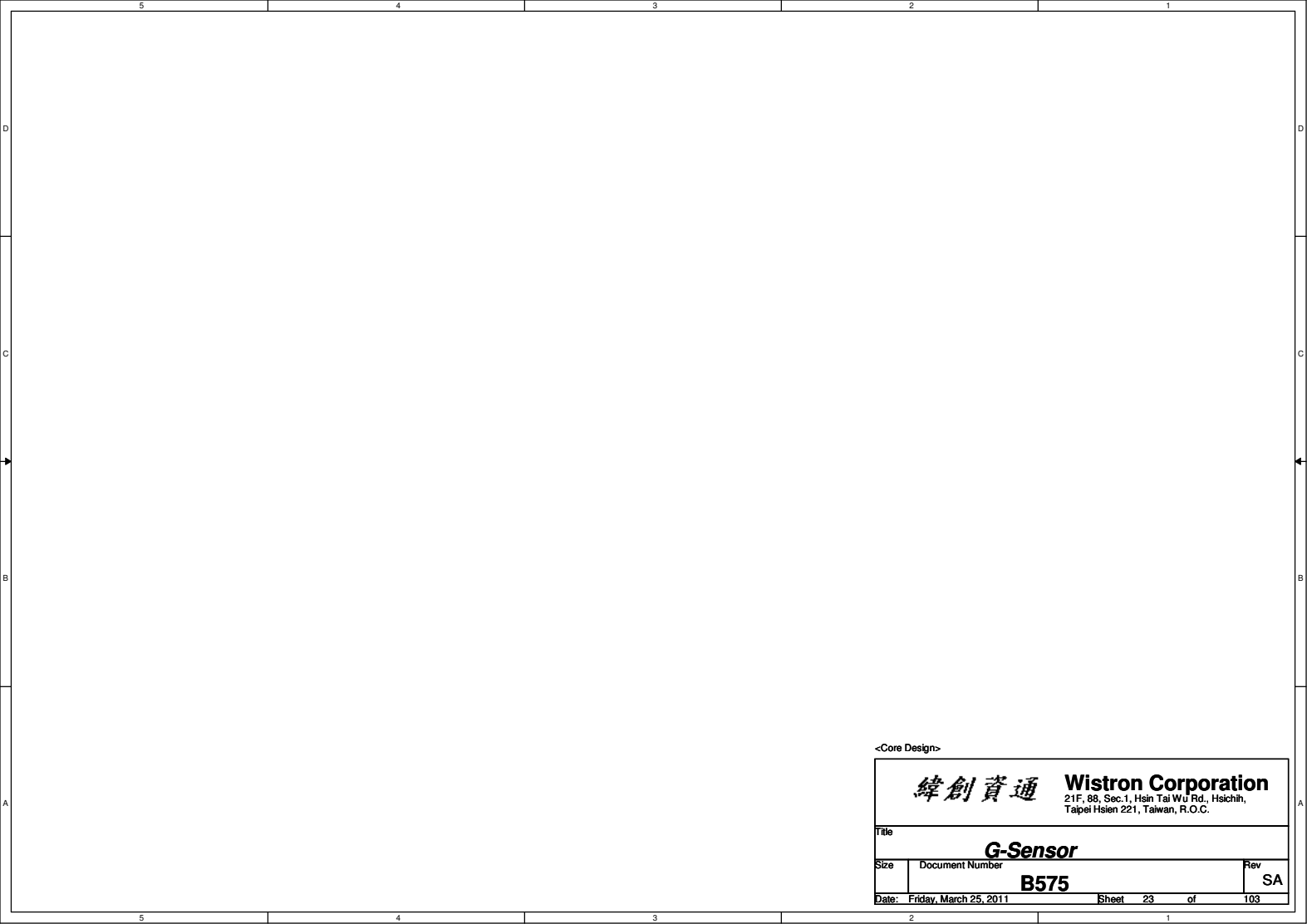
Note: FCH has 15K internal PU FOR PCI_AD[27:23]

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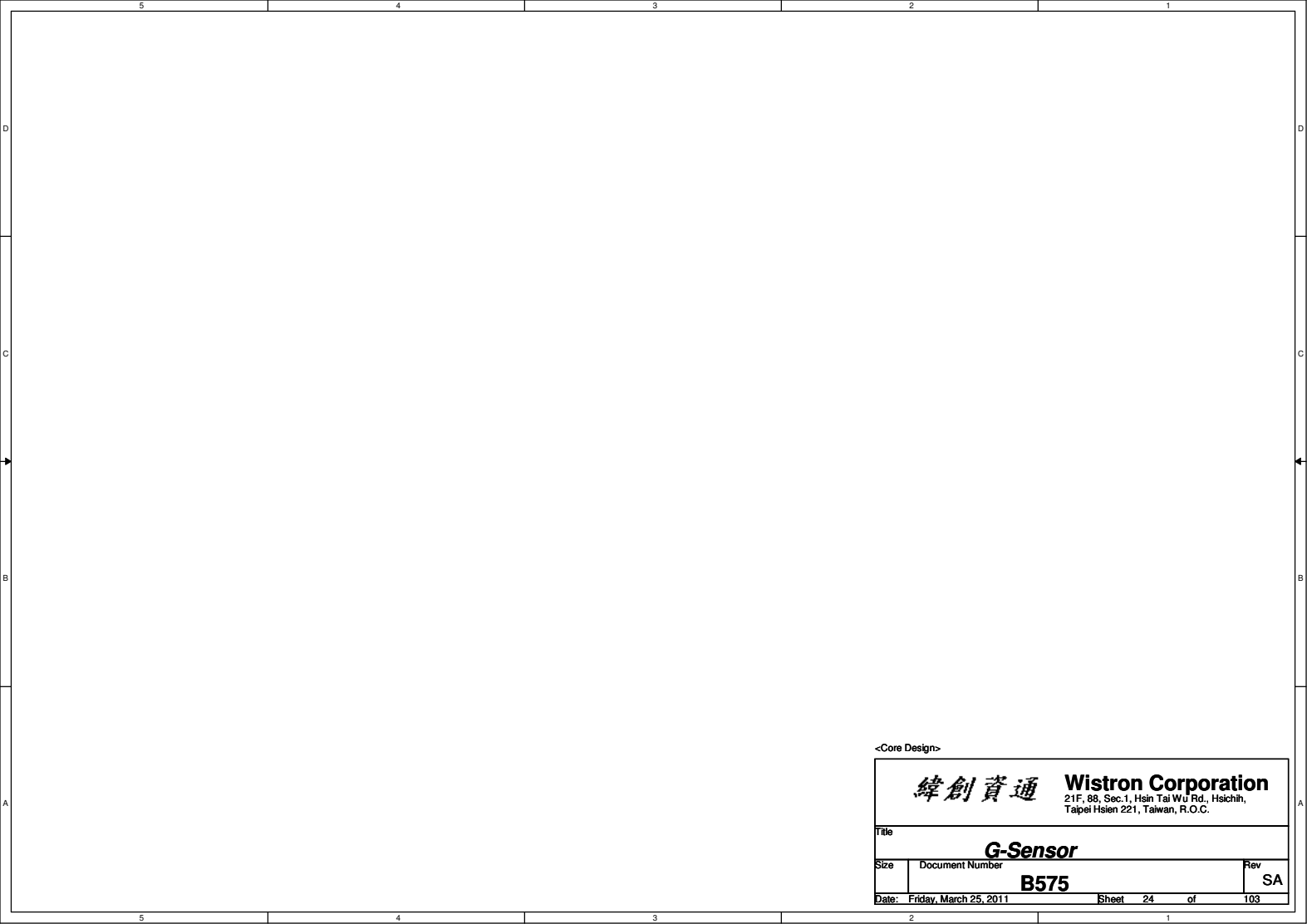
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File FCH 6 of 6(VSS)		
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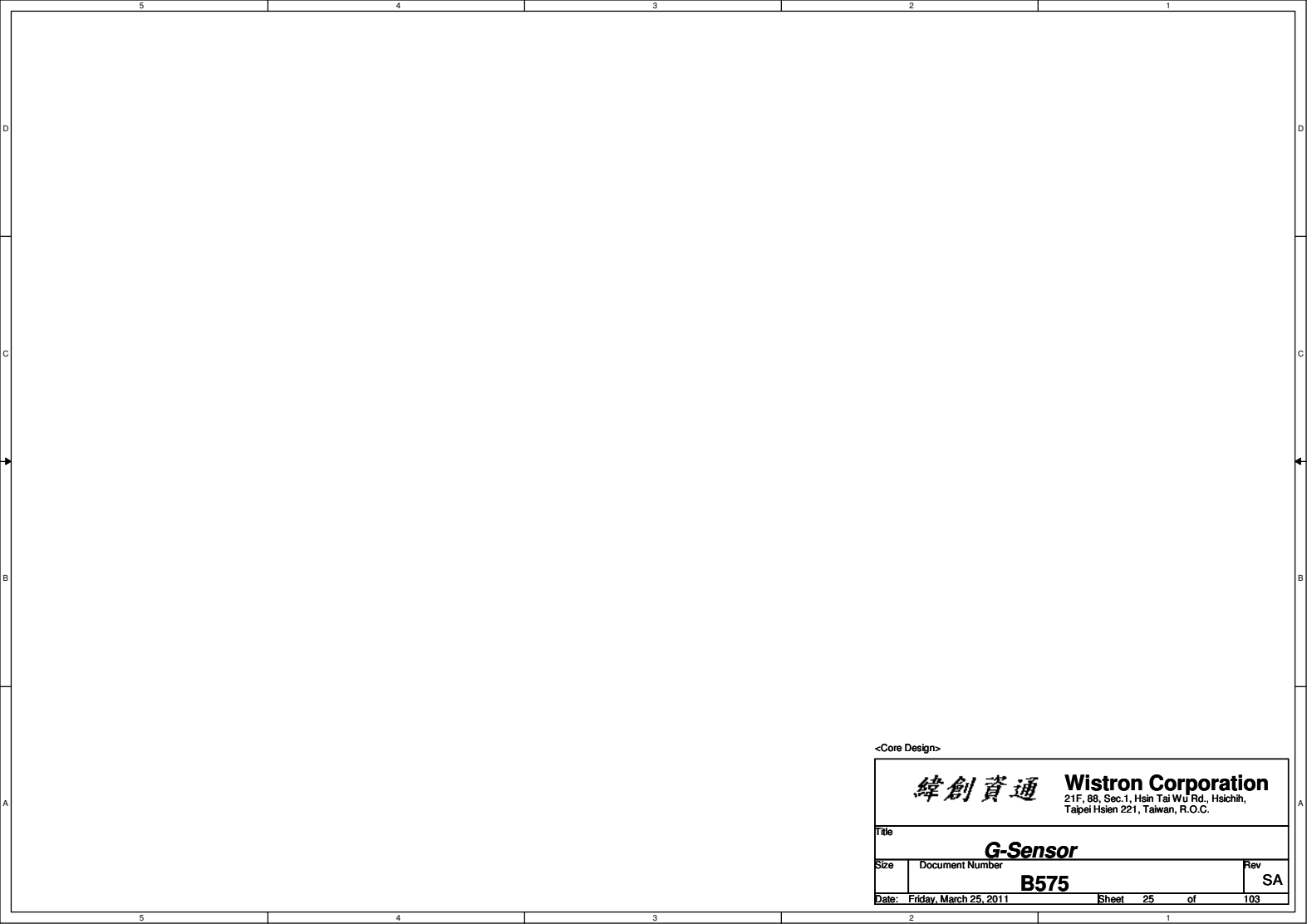
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File

Power Button

Size
A3

Document Number
B575

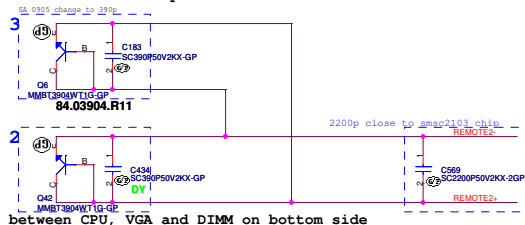
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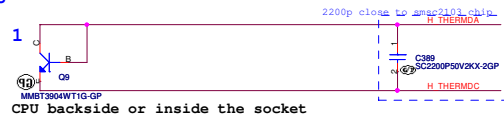
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Close to PCH on top side.



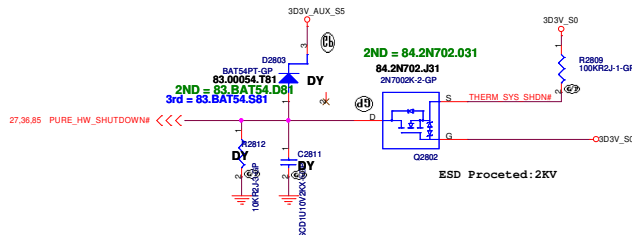
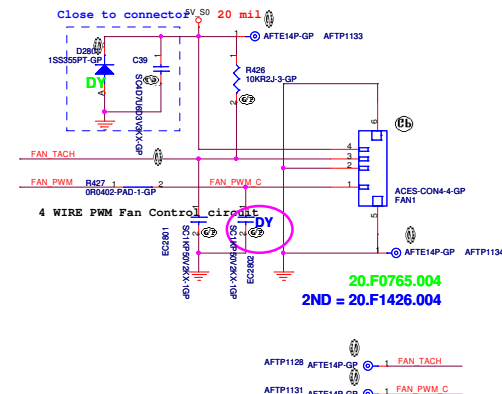
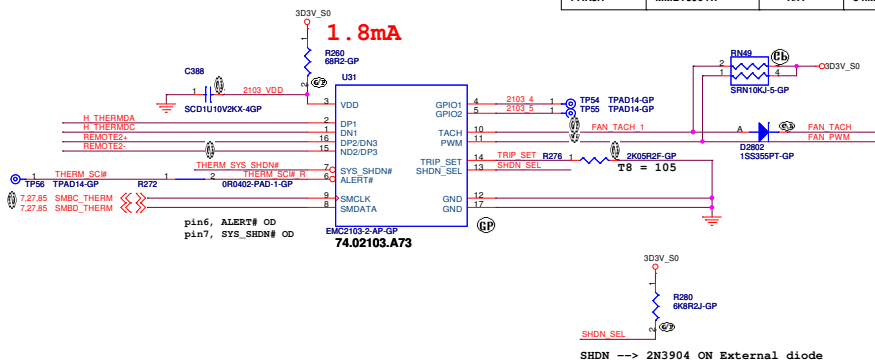
T8



CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Table 28.1- General Purpose Transistors multi-source

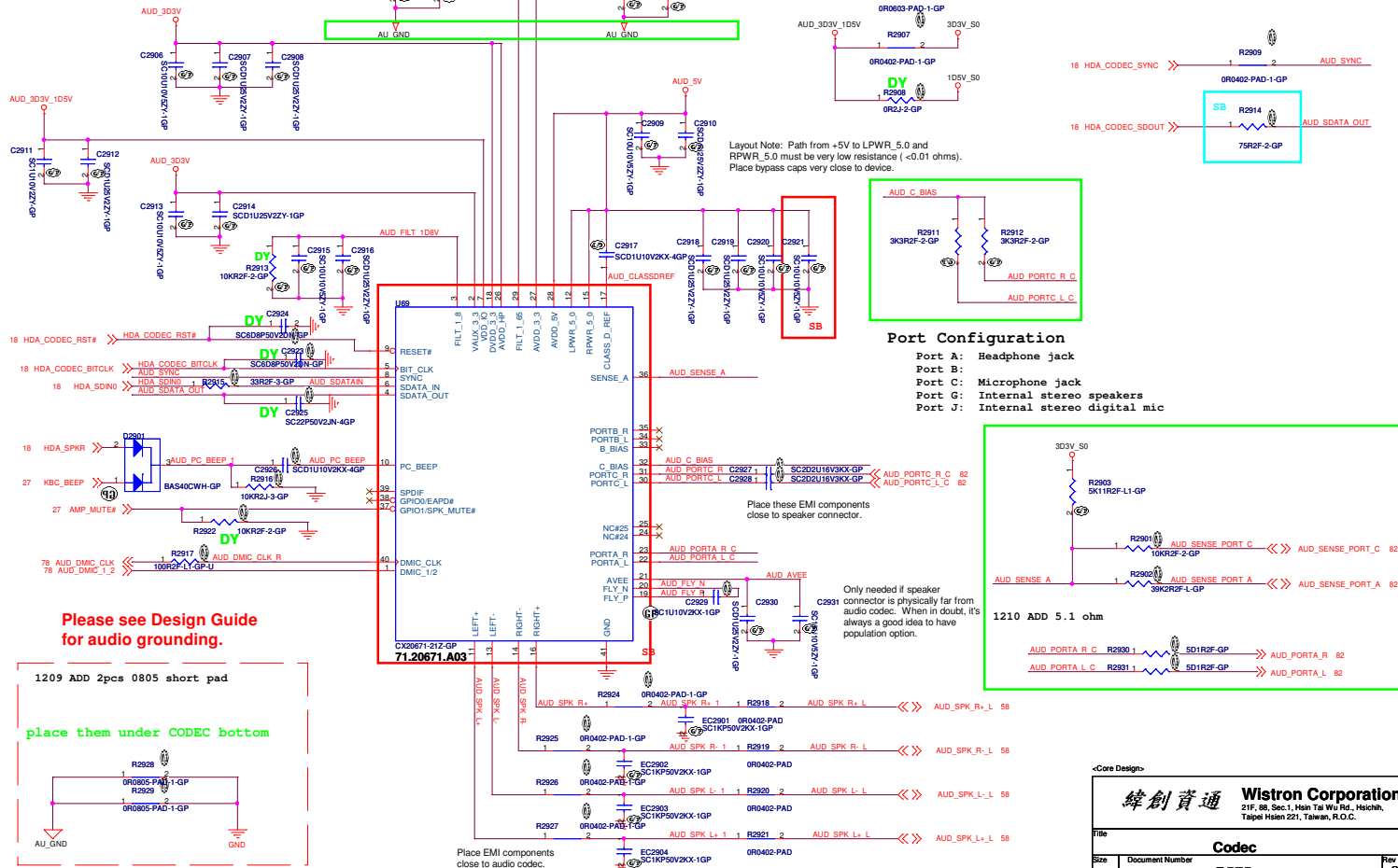
Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11



Core Design

1210 10886-1 D1/D2/R15/R16/C15 DY
EC1/EC2/EC3 100pF
R17/R18 100ohm
C17/C18 100pF
R23/R24 100pF

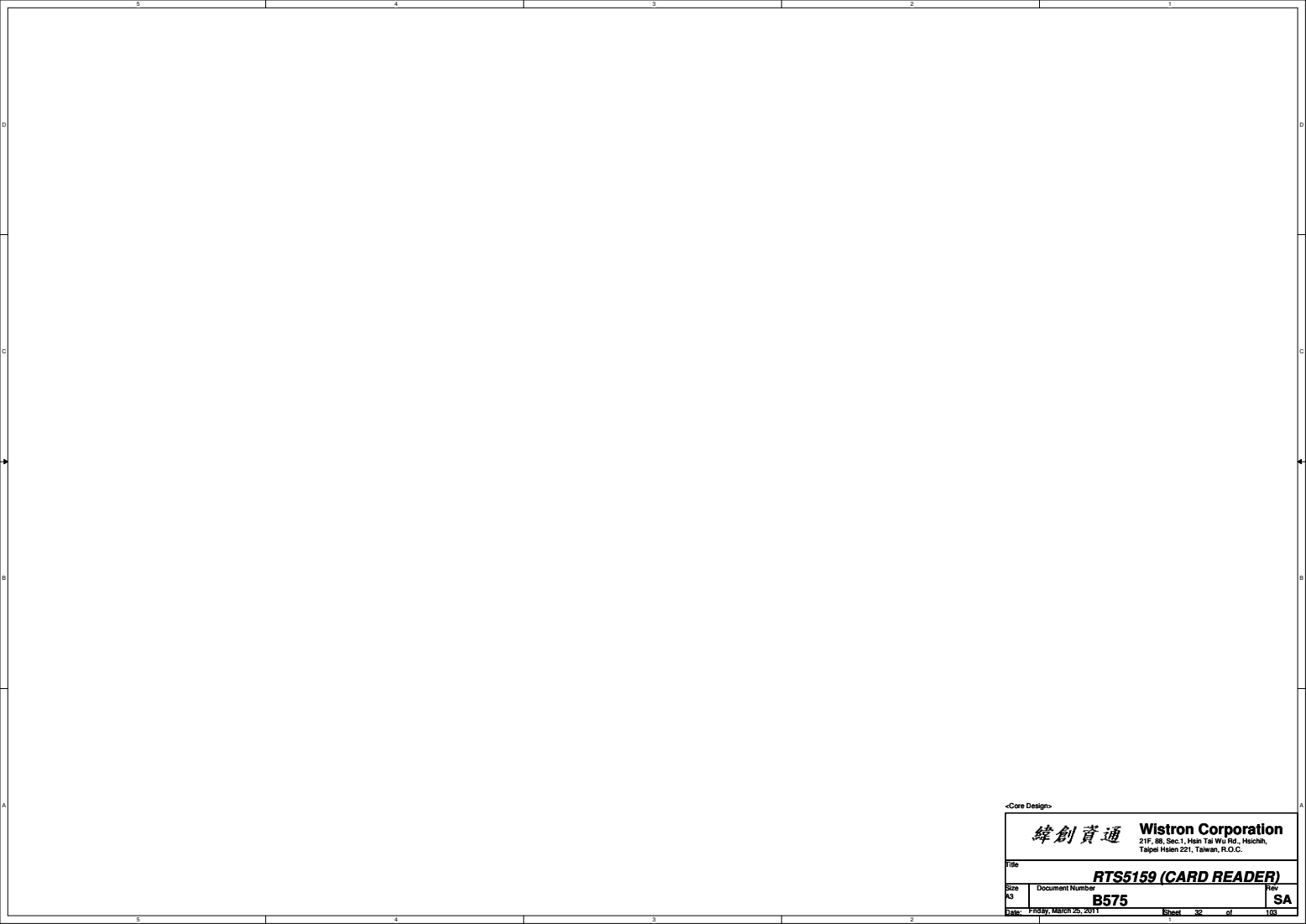
BOM Control



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LA57 UMA

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RTS5159 (CARD READER)			
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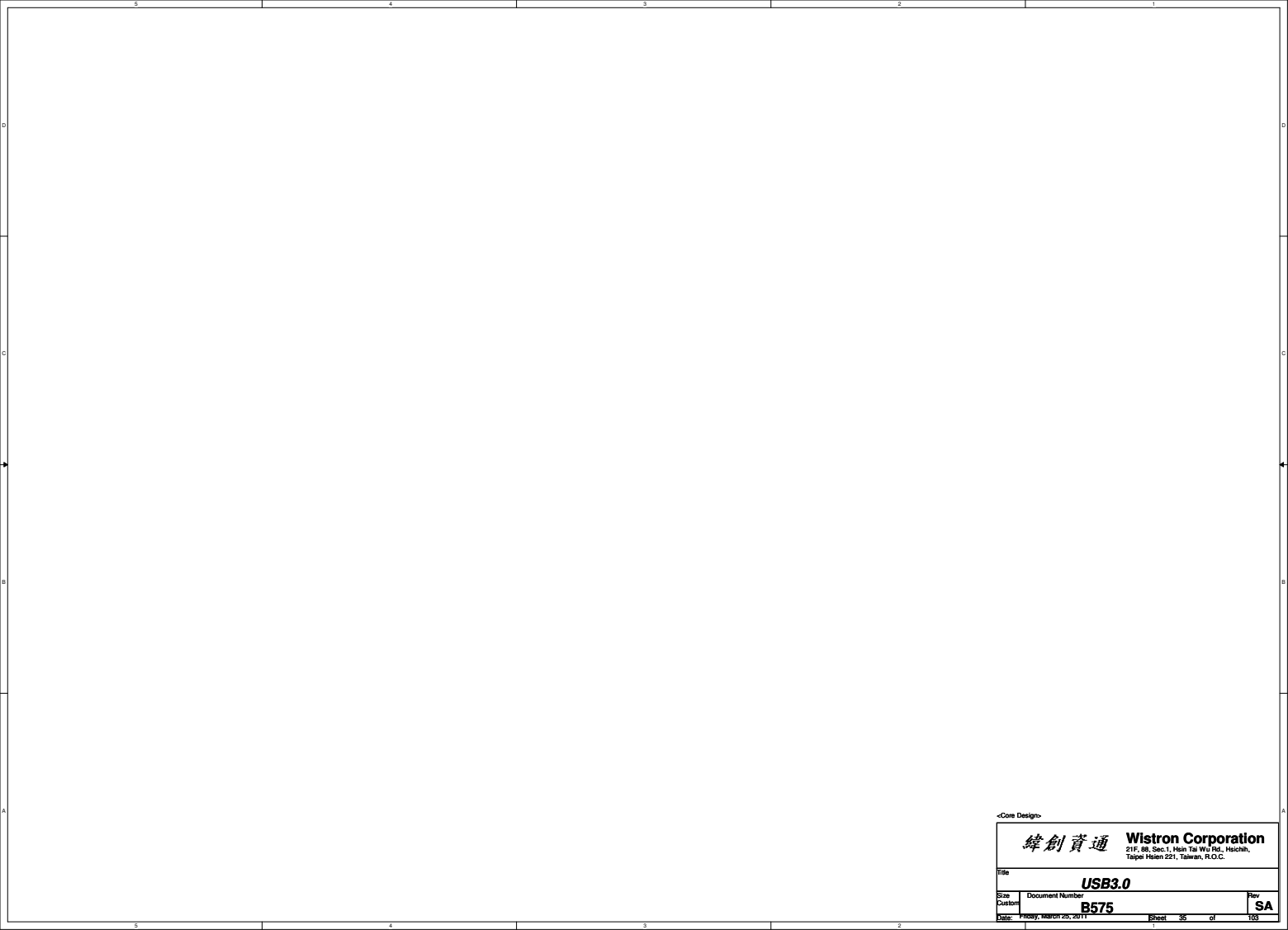
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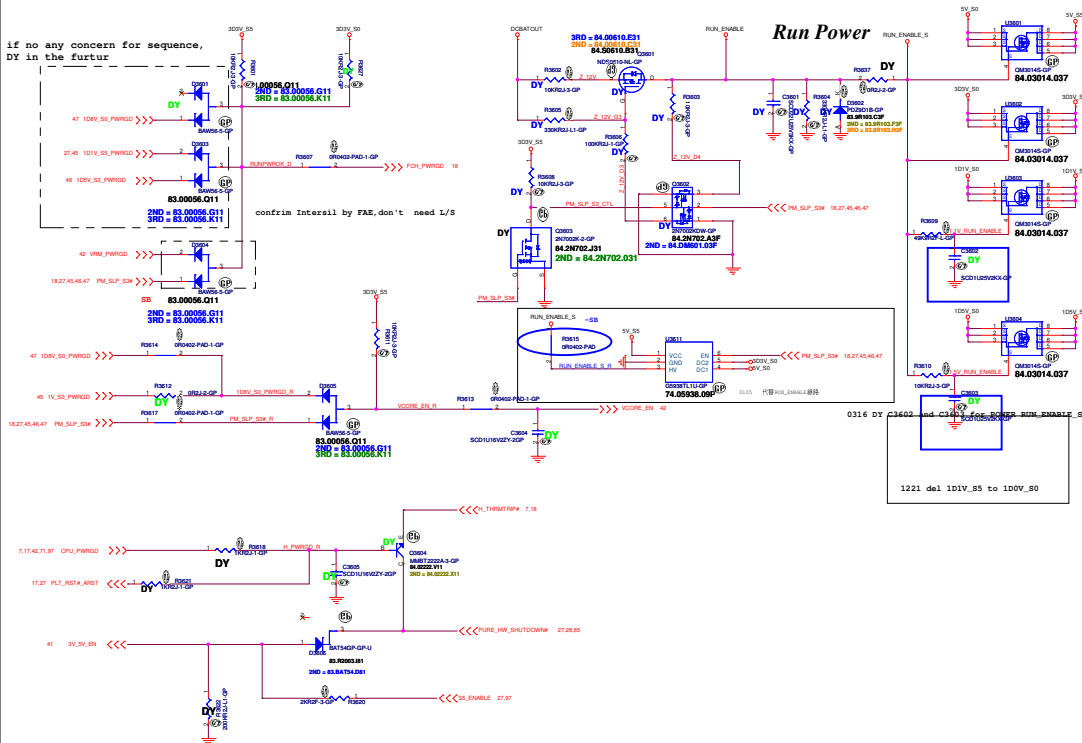
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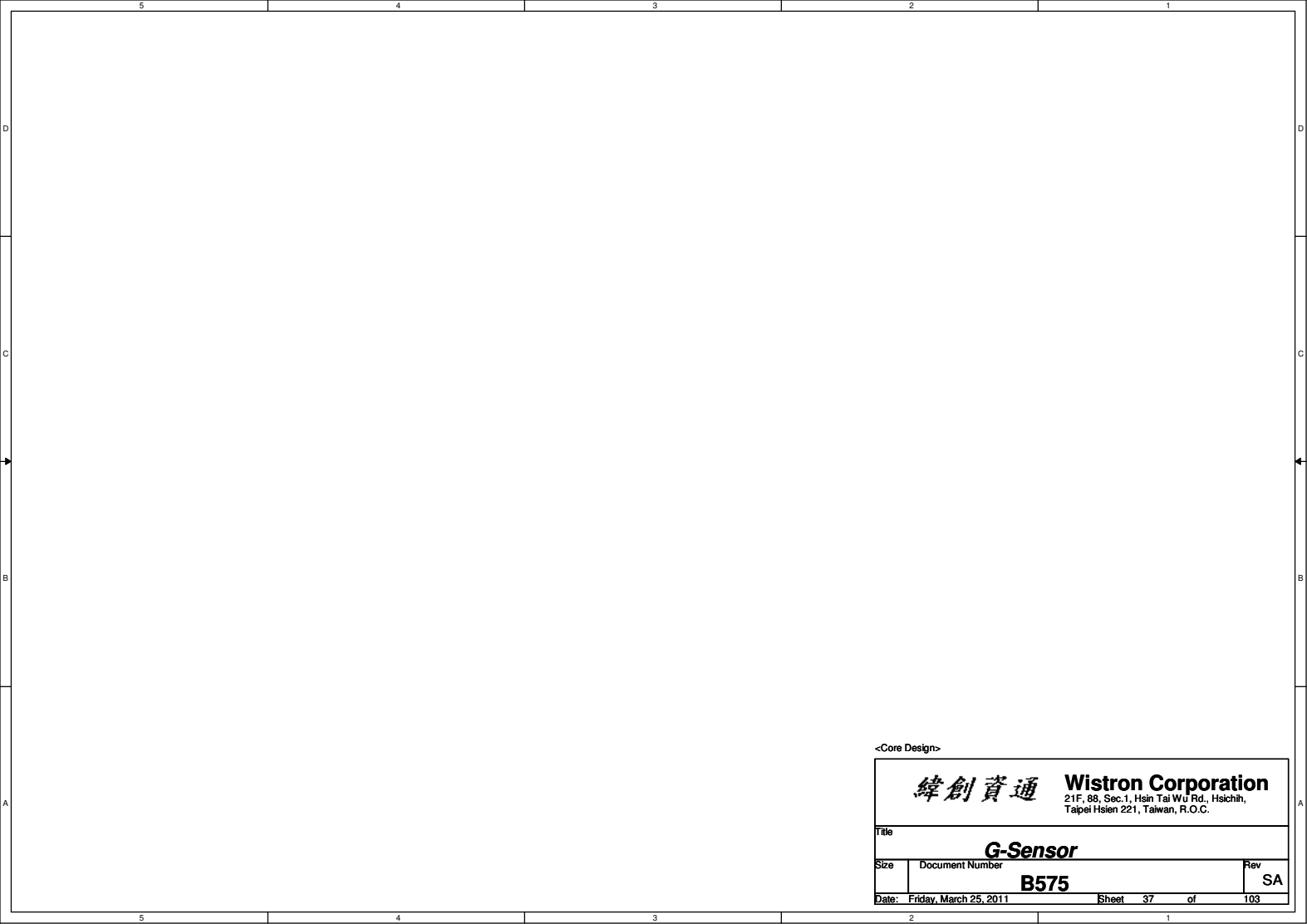
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USB3.0			
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if no any concern for sequence,
DY in the futur



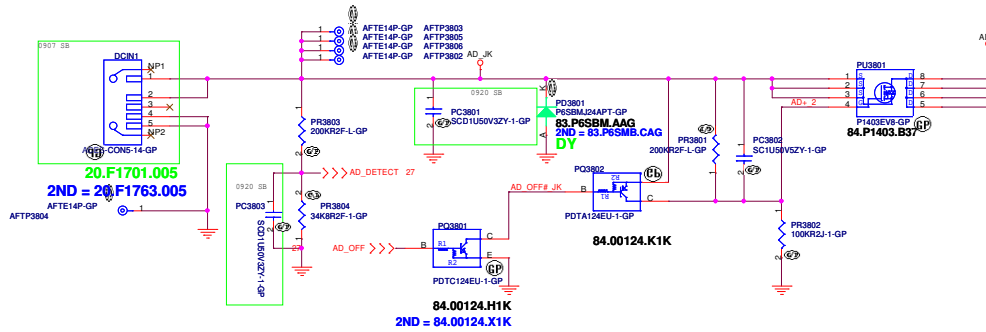
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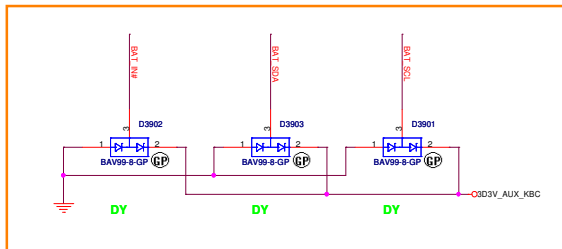
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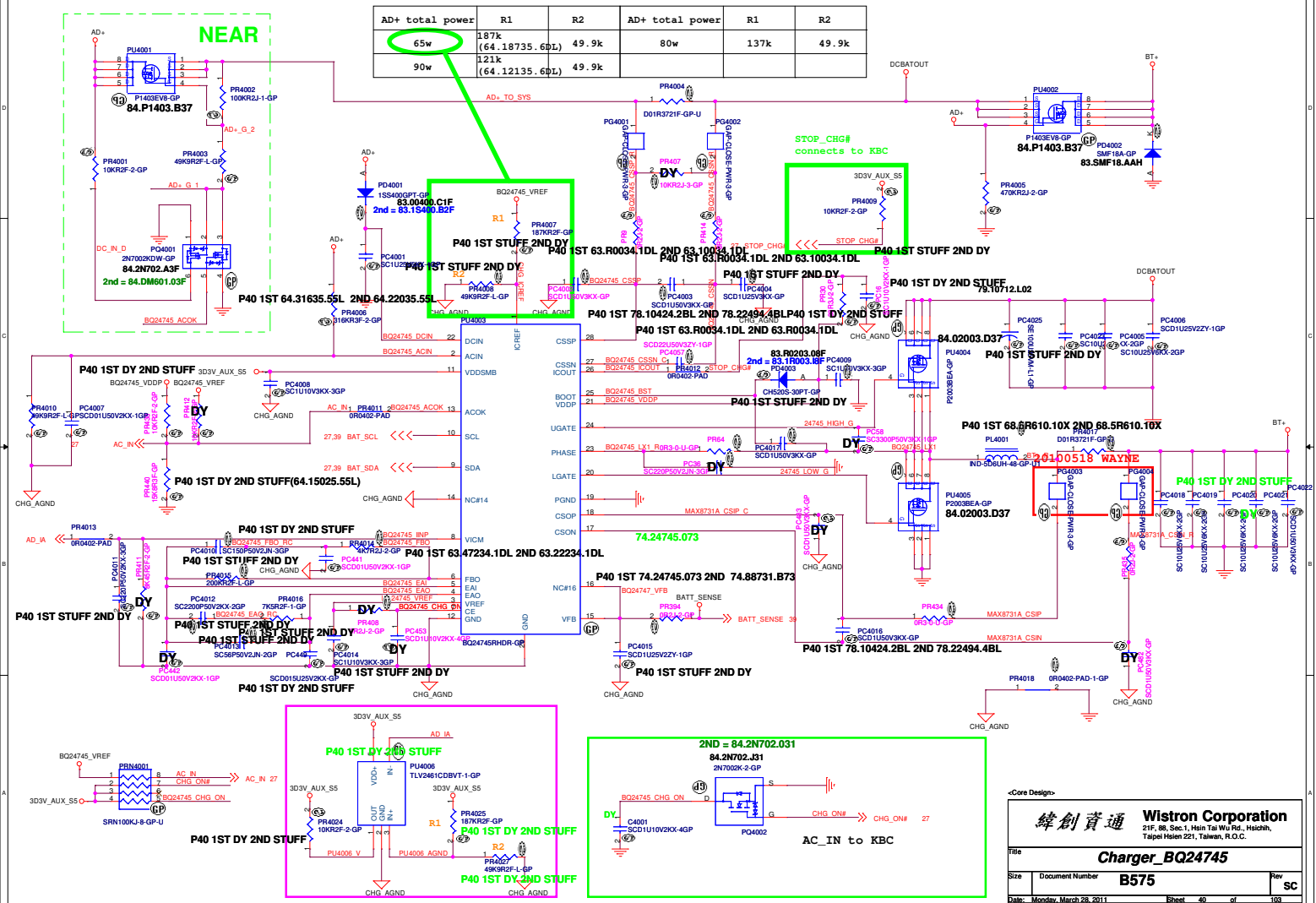
Adaptor in to generate DCBATOUT



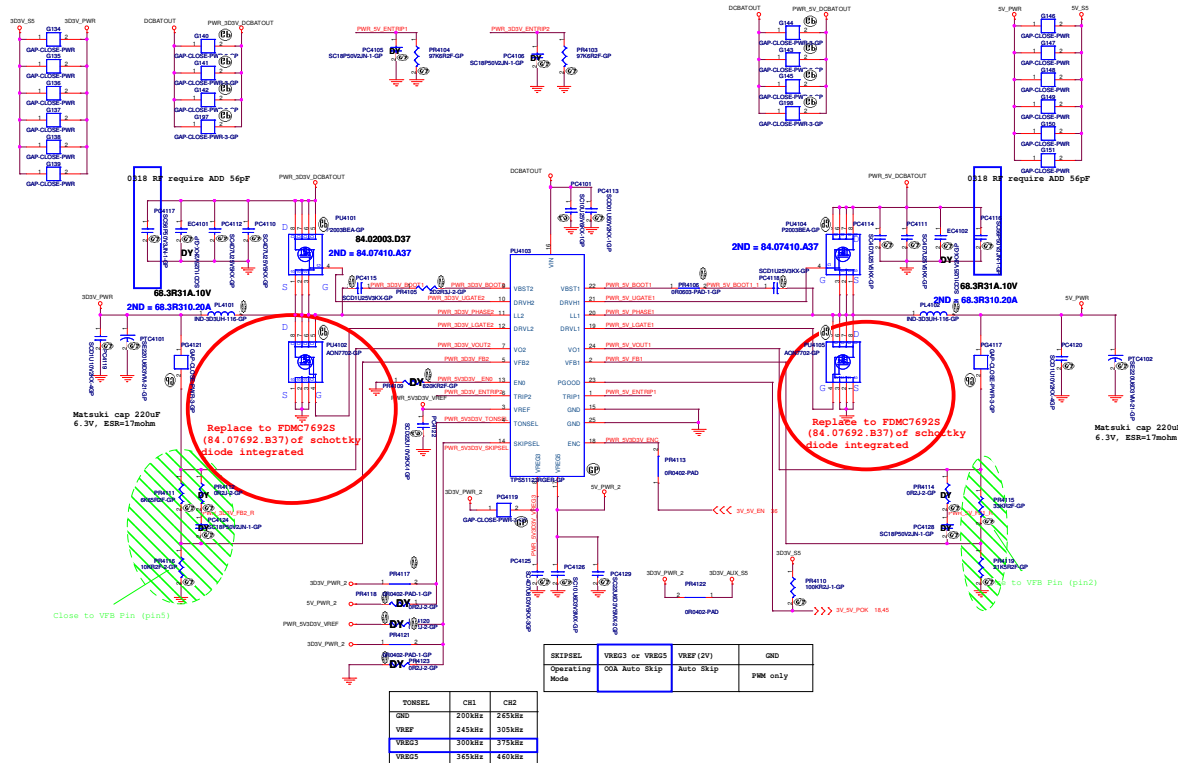
JV10-CS



AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6BL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6BL)	49.9k			

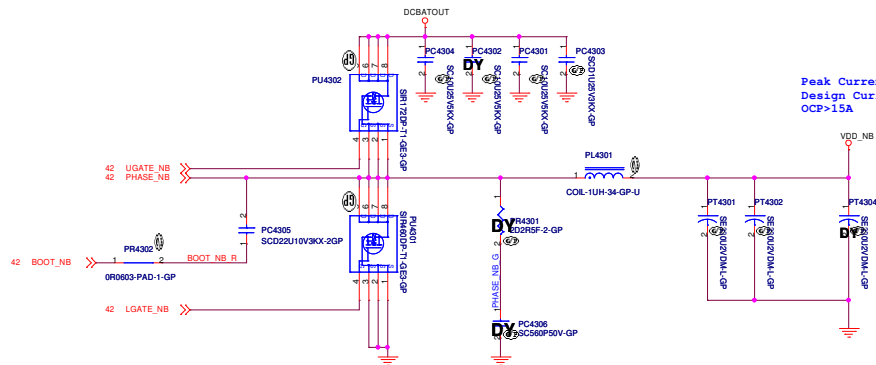


SSID = PWR.Plane.Regulator_5v3p3v



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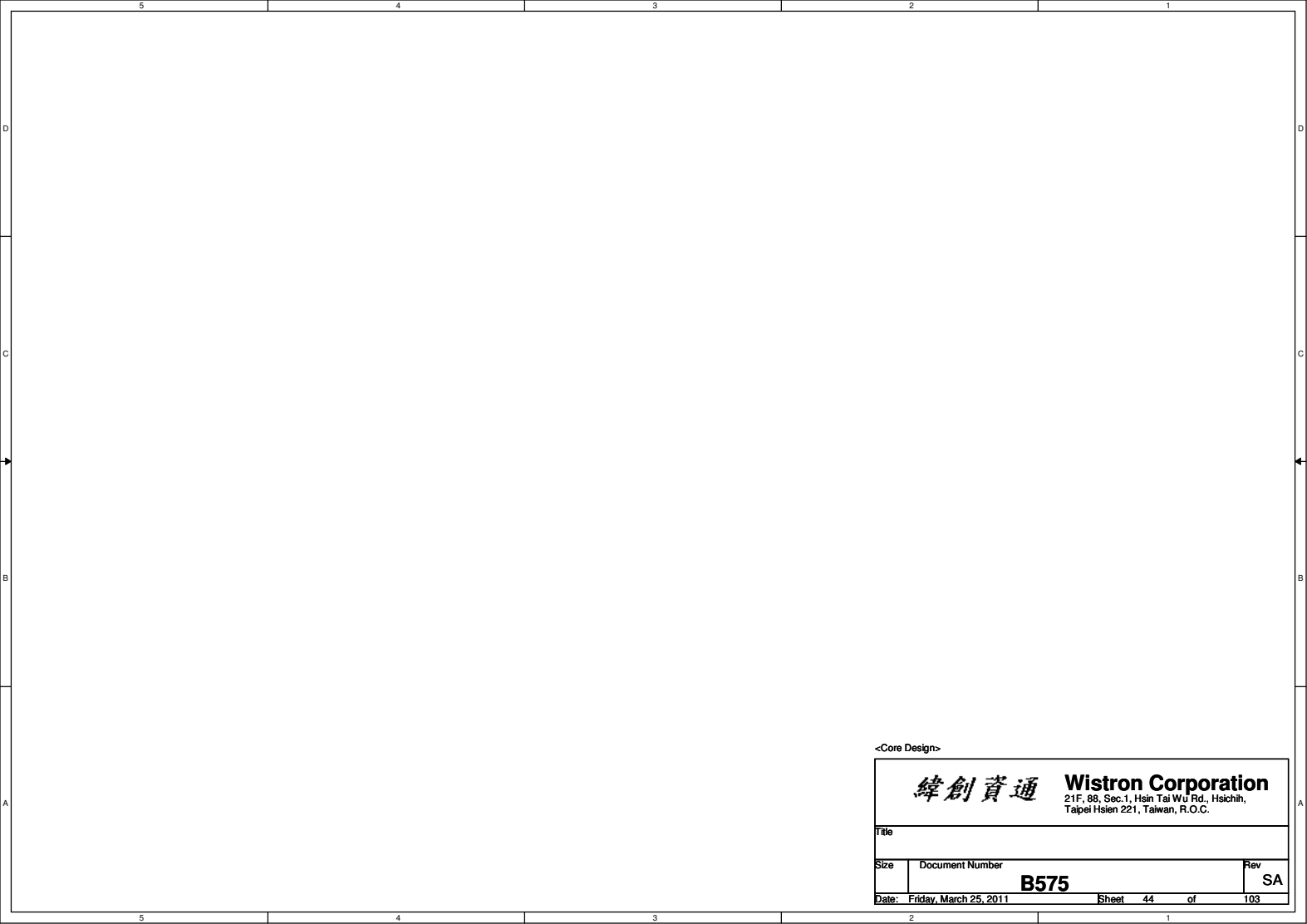


Peak Current=10
Design Current =8A
OCP>15A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat -22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR712DF/ POWERPAK/ 10.3mOhm/ 12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR460DF/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

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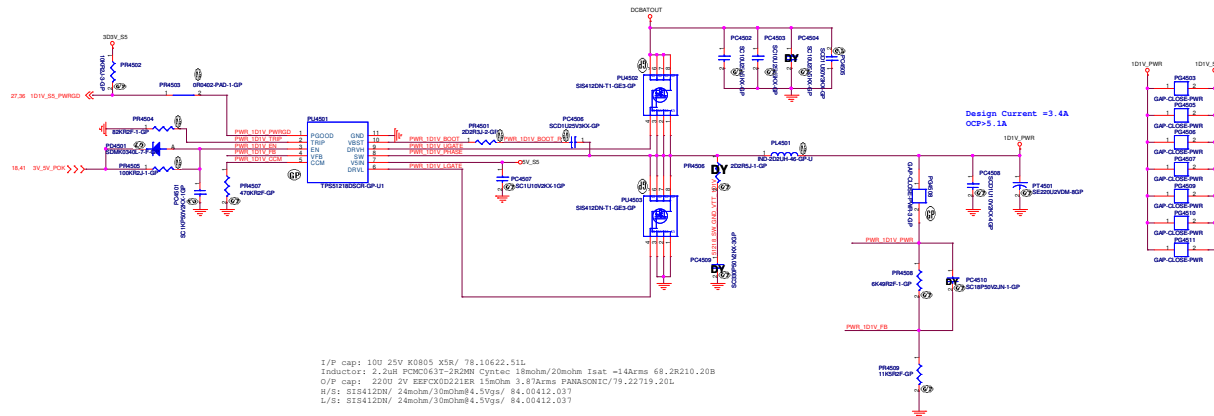
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		VREG_VDDNB	
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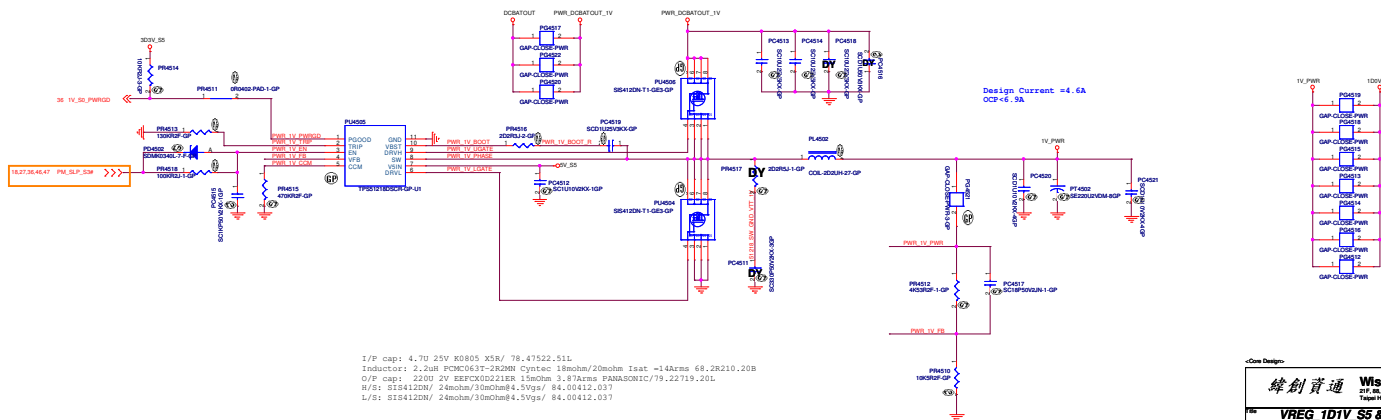
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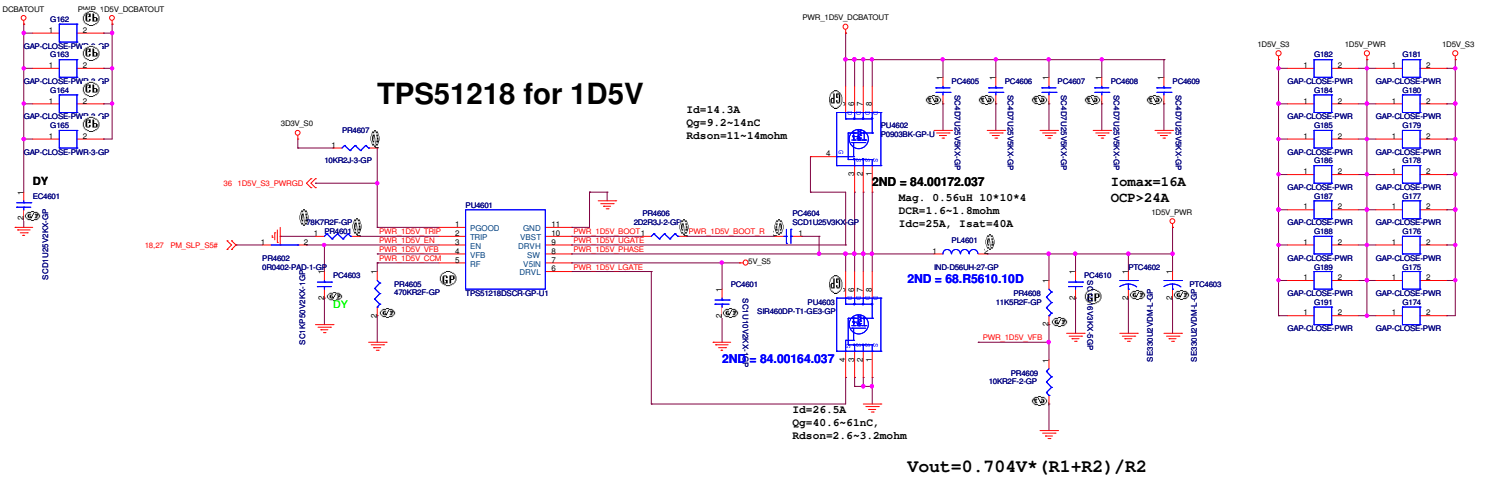
I/P cap: 100 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R20M Cynotec 18mohm/20mohm Isat ~14Arms 68.2R210.20B
O/P cap: 2200 2V KEEPCX02218 15mOhm 3.8Arms PANASONIC/79.22719.20L
H/S: S1S412DN/ 24mohm/30mohm@4.5Vgs/ 84.00412.037
L/S: S1S412DN/ 24mohm/30mohm@4.5Vgs/ 84.00412.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

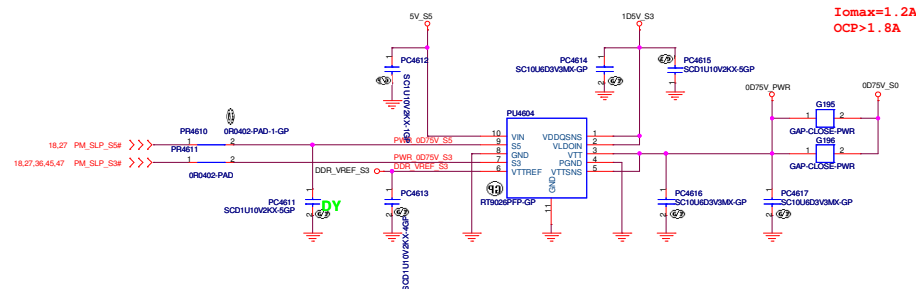


I/P cap: 4.7u 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R20M Cynotec 18mohm/20mohm Isat ~14Arms 68.2R210.20B
O/P cap: 2200 2V KEEPCX02218 15mOhm 3.8Arms PANASONIC/79.22719.20L
H/S: S1S412DN/ 24mohm/30mohm@4.5Vgs/ 84.00412.037
L/S: S1S412DN/ 24mohm/30mohm@4.5Vgs/ 84.00412.037

Clone Design



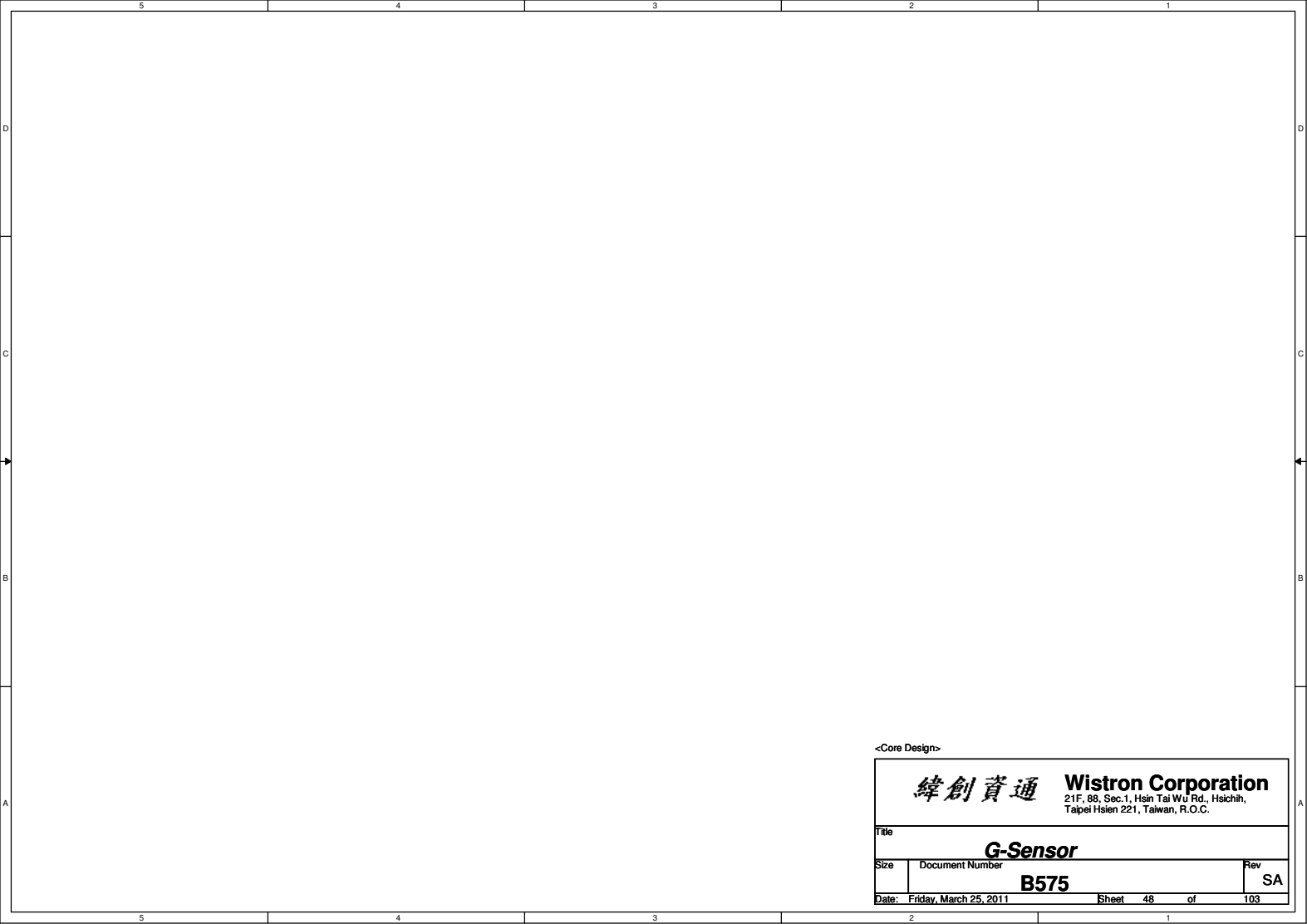
RT9026 for 0D75V_S3




©Core Design

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichai,
Taipei Hsien 221, Taiwan, P.O.C.



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
G-Sensor			
Size	Document Number		Rev
	B575		SA
Date: Friday, March 25, 2011		Sheet 48	of 103

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(Blanking)

<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,</div>		<div>Tapel Hsien 221, Taiwan, R.O.C.</div>	
Title			
S-VIDEO			
Size	Document Number		Rev
A4	B575		SA
Date:	Friday, March 25, 2011		Sheet 53 of 103

(Blanking)

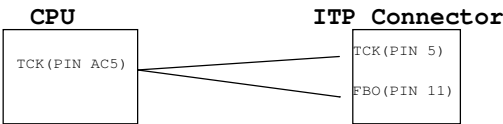
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.</div>	
Title	
Reserved	
Size	Document Number
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

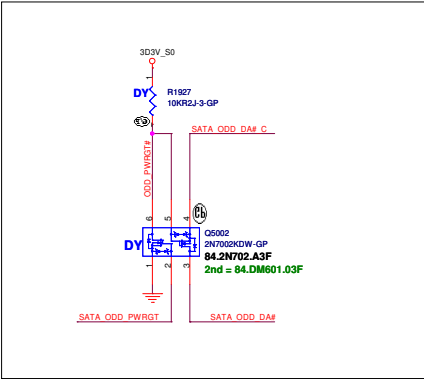
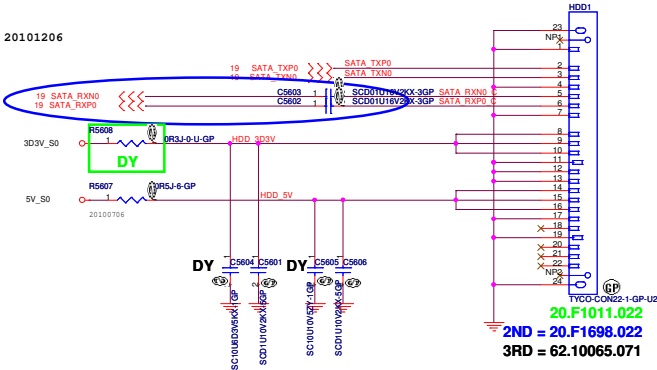


<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ITP			
Size	Document Number		Rev
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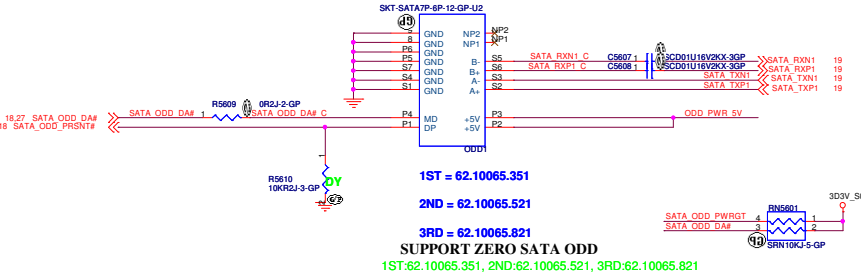
SATA HDD Connector

20101206

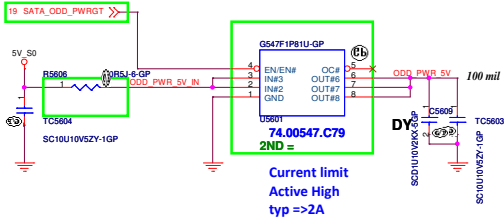


ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil
Mars:
Exchange ODD and ESATA differential pair each other.

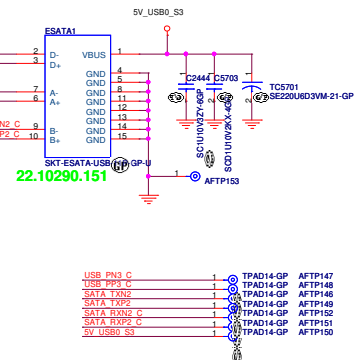
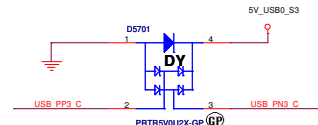
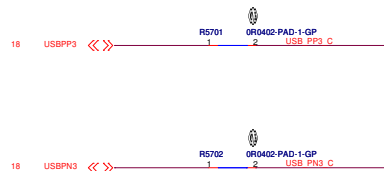


SATA Zero Power ODD



Current limit
Active High
typ =>2A

<Core Design>



29 AUD_SPK_L+L <<>>
29 AUD_SPK_L+L <<>>

Place these EMI components
close to speaker connector.

Only needed if speaker
connector is physically far from
audio codec. When in doubt, it's
always a good idea to have
population option.

EC5801 SC100P50V2JN-3GP
EC5802 SC100P50V2JN-3GP

20100723 change



2ND = 20.F0693.002

1ST = 20.F1240.002

1ST:20.F1240.002, 2ND:20.F0693.002



2ND = 20.F0693.002

1ST = 20.F1240.002

1ST:20.F1240.002, 2ND:20.F0693.002

AFTP138 AFTE14P-2 1 AUD_SPK_L+L
AFTP137 AFTE14P-2 1 AUD_SPK_L+L
AFTP129 AFTE14P-2 1 AUD_SPK_R+L
AFTP140 AFTE14P-GP 1 AUD_SPK_R+L

29 AUD_SPK_R+L <<>>
29 AUD_SPK_R+L <<>>

EC5803 SC100P50V2JN-3GP
EC5804 SC100P50V2JN-3GP

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File		Rev
SPEAKER		SA
Size	Document Number	
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Date:	Modified: March 28, 2011	Sheet 58 of 100

Reserved

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 321, Taiwan, R.O.C.

File

Reserved

Size
A3

Document Number
B575

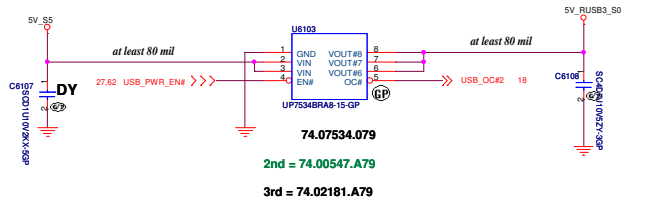
Date: Friday, March 25, 2011

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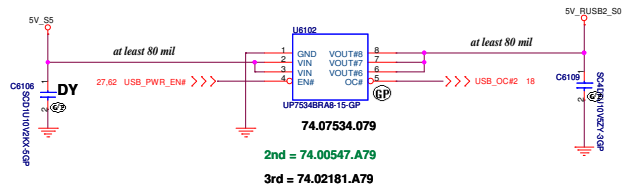
Rev
SA

SSID = USB

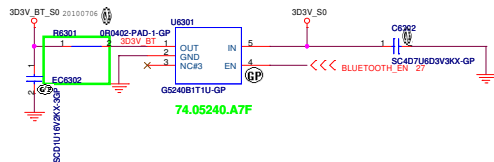
RJ45_USB Board USB Power



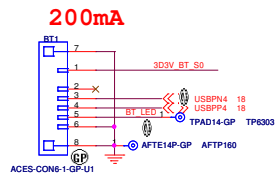
I/O Board USB Power



BT CONN.

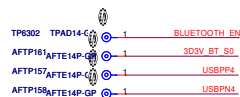


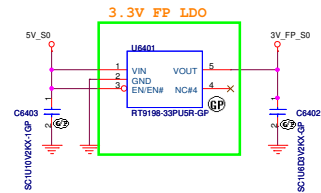
EC6302 put near
BLUE1 / all USB
put one choke
near connector
by EMI request



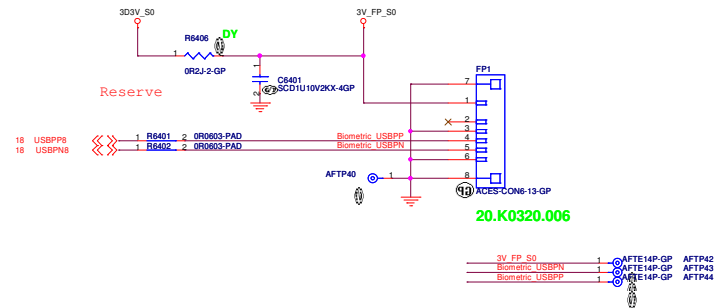
20.F0772.006

2ND = 20.F1804.006



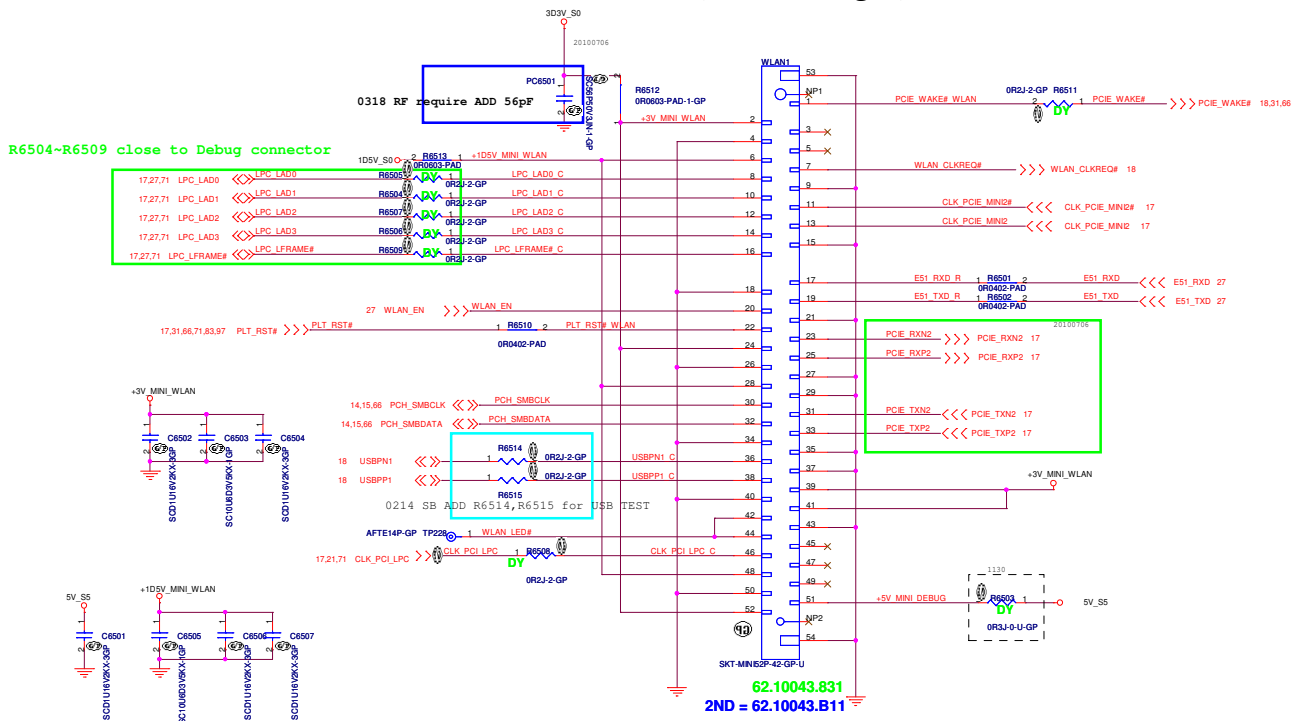


Finger Printer Connector



SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File

MINICARD WLAN

Size

Document Number

Rev

B575

SA

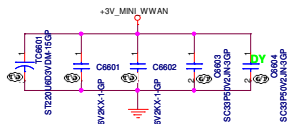
Date: Monday, March 28, 2011

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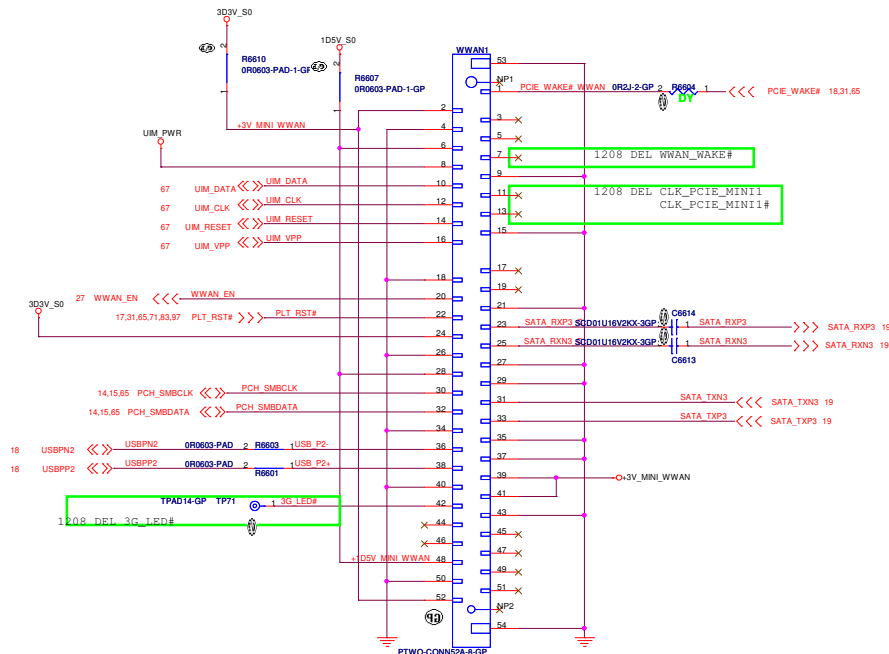
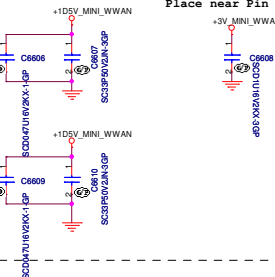
SSID = Wireless

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 321, Taiwan, R.O.C.

File

MINICARD_WWAN

Size

Document Number

Rev

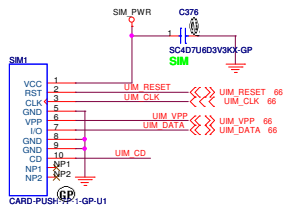
B575

SA

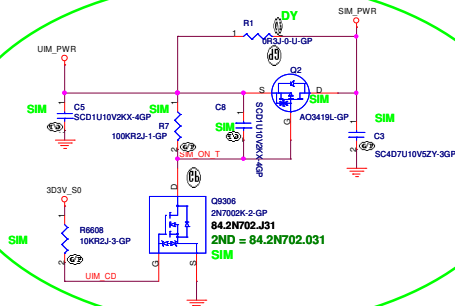
Date: Monday, March 28, 2011

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SIM



20.10073.001



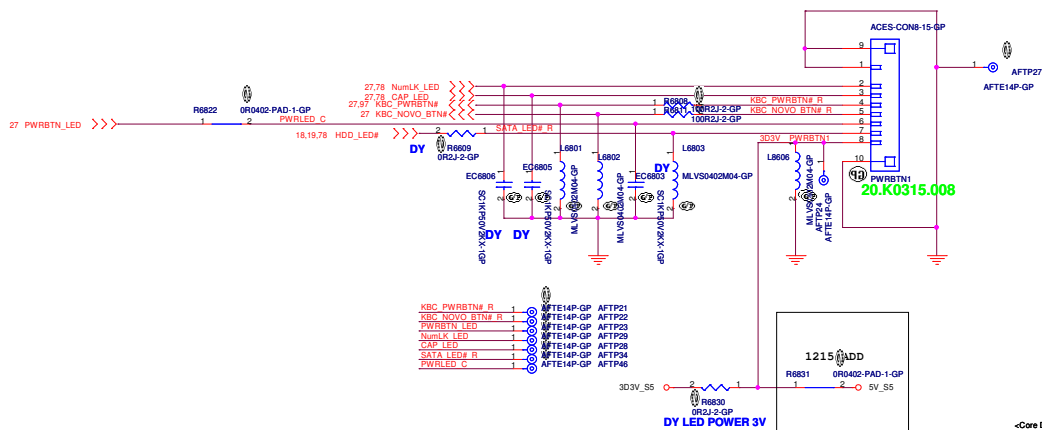
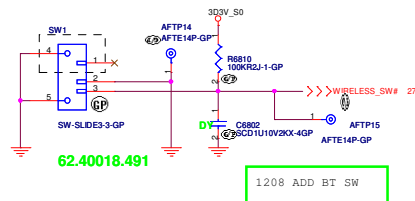
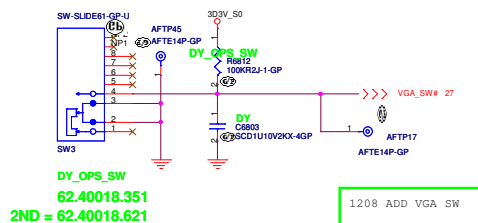
<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File		SIM CARD	
Size	Document Number	B575	
A3		SA	
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```
SSID = User.Interface
```



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Item	Value
1. Title	

Size

Document Number

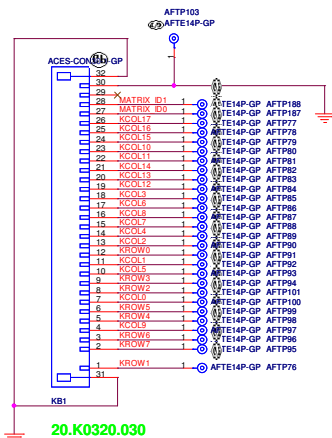
POWER BUTTON

B575

Rev

Date: Monday, March 28, 2011 Sheet 68 of 103

Internal KeyBoard Connector



S205少兩PIN,
原為測點已補上

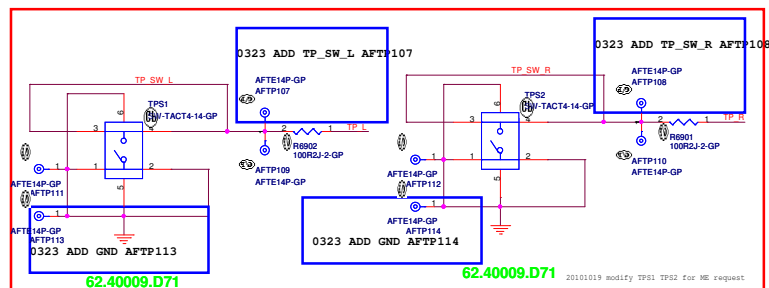
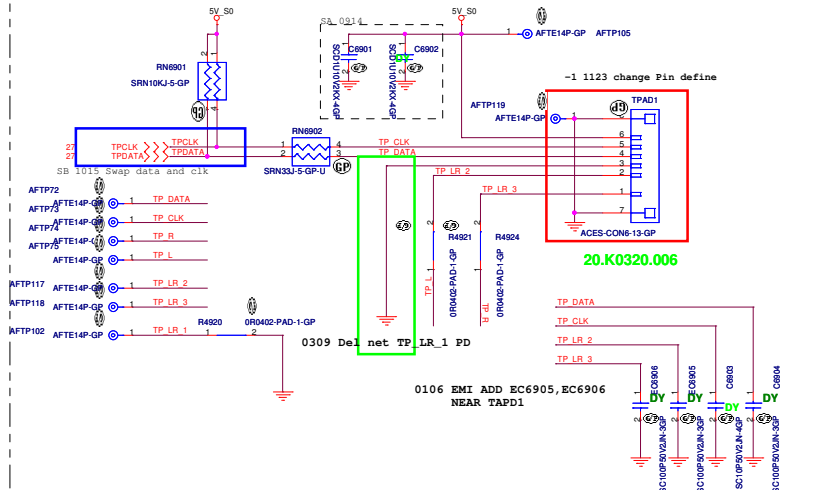
ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

—<> KROW[7..0] 27

— <> KCOL17.0] 27

20.K0320.030

```
SSID = Touch.Pad
```



20101019 modify TPS1 TPS2 for ME request

•Core Design:

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

KB/TP CONN

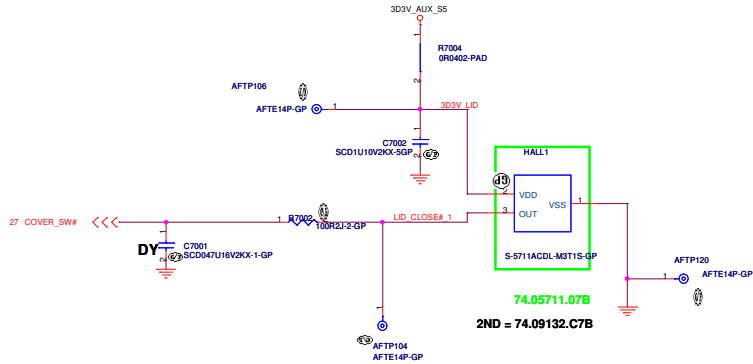
Size

Document Number

Rev

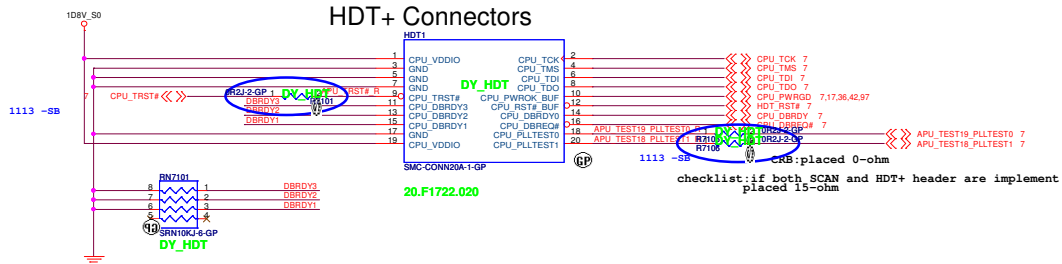
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Hall Sensor

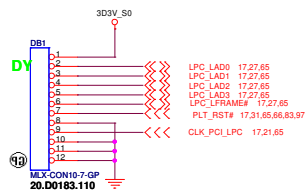


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File		Wistron Corporation	
Size		21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Document Number		HALL Sensor	
Date: Monday, March 28, 2011		Rev SA	
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GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

緯創資通		Wistron Corporation	
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.		21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
Debug Port			
Size	Document Number		Rev
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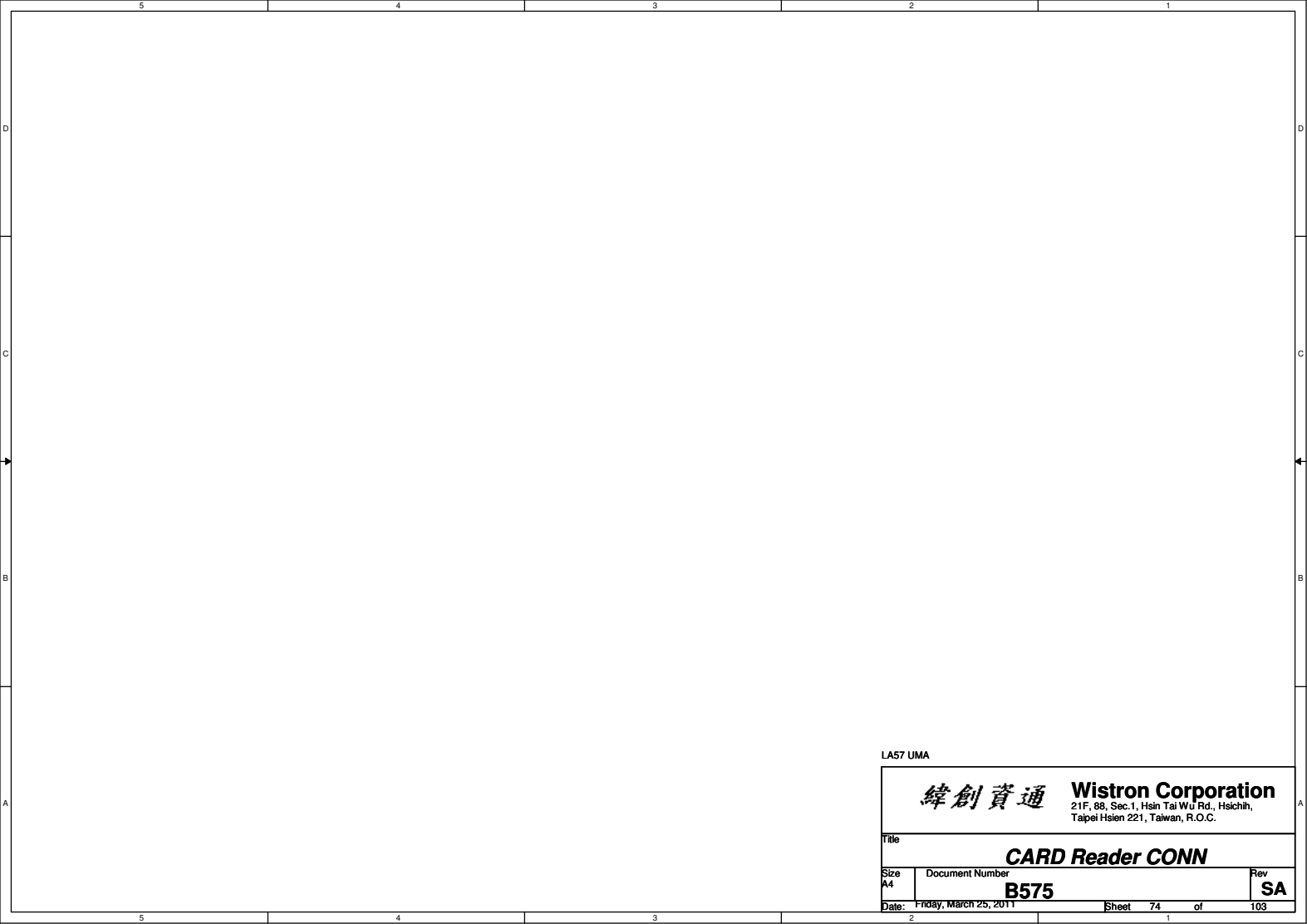
LA57 UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
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(Blanking)

LA57 UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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5 4 3 2 1

D

D

C

C


B

B

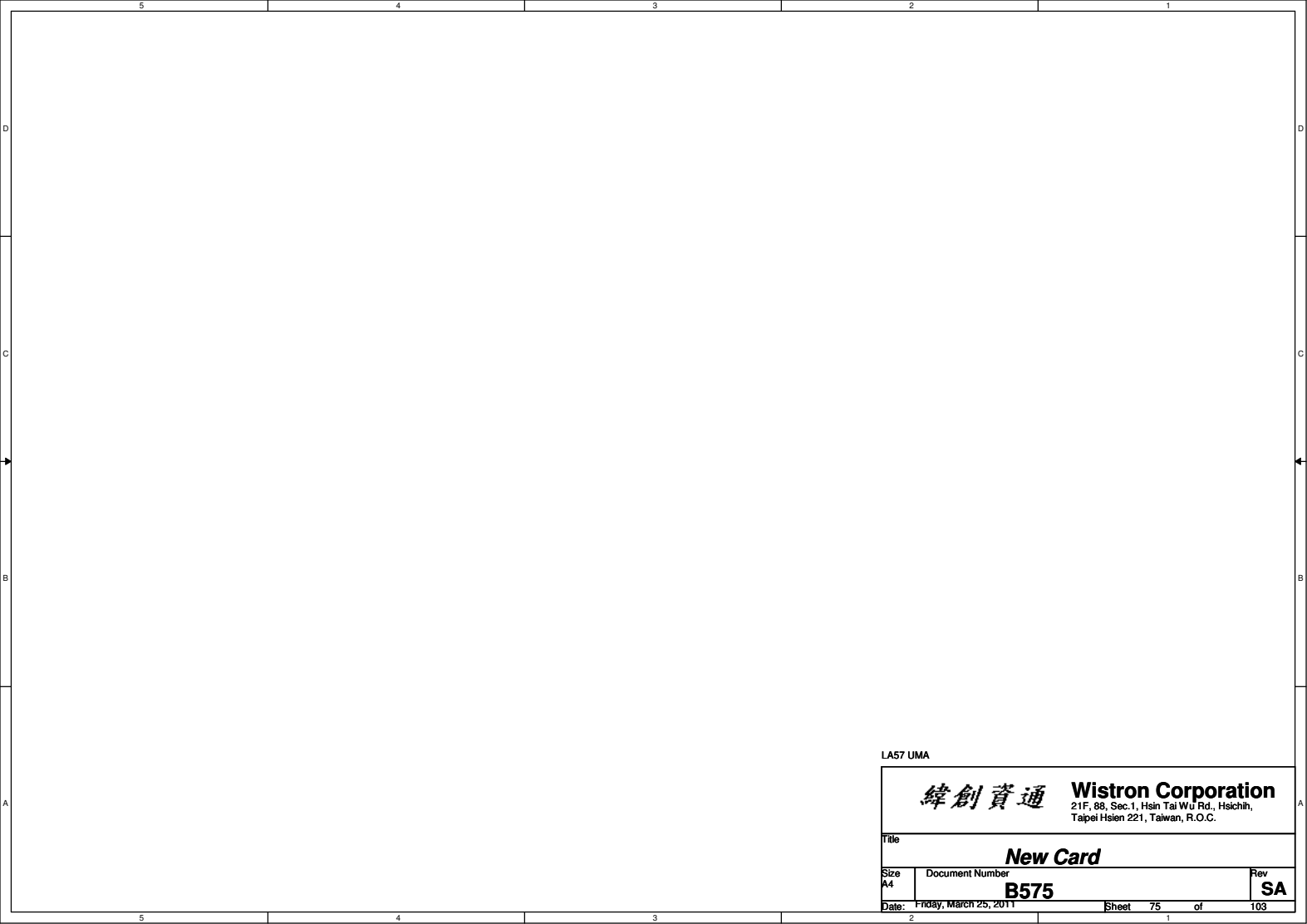
A

A

LA57 UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CARD Reader CONN			
Size	Document Number		Rev
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5 4 3 2 1



LA57 UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
<i>New Card</i>			
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LA57 UMA

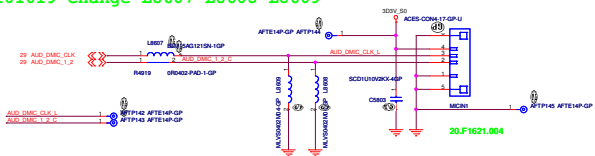
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
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Reserved			
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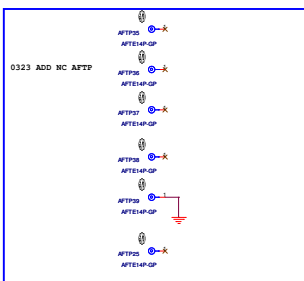
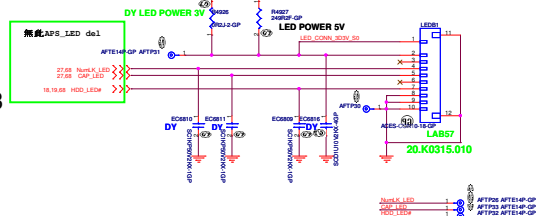
LA57 UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Tapei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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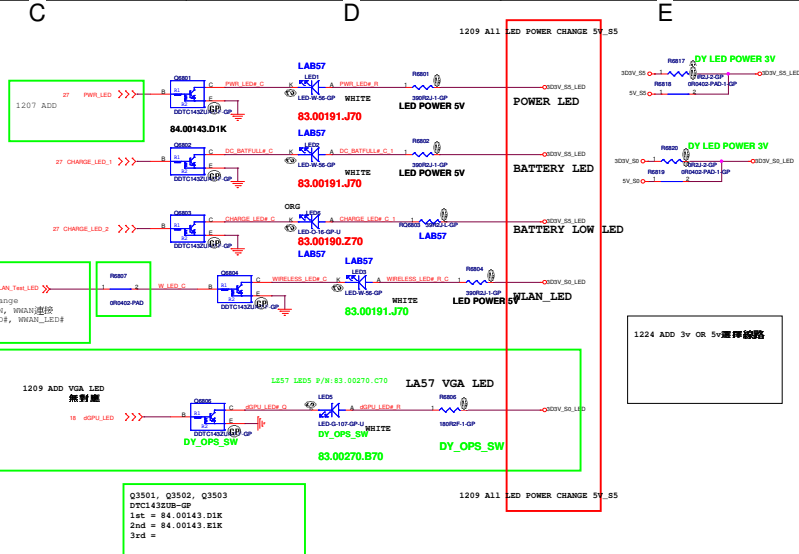
20101019 change L8607 L8608 L8609



LED BORD CONN.



LED



Core Design

緯創資通

Wistron Corporation

21F, 8th, Sec. 1, Hsin-Tai Wu Rd., Hsinshu,

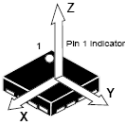
Taichung 405, Taiwan, R.O.C.

REFERENCE		SA
Doc No.	Document Number	
Rev.	B575	100
Date: Monday, March 24, 2014		

	ADXL322	
	LIS244AL	No Accel
	LIS34AL	
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

Layout Comment :
(1) Place C483, C484, Q46, R528, R530,
C479, C476, R509, R508 close to U55.
(2) Avoid routing under DCDC switching area.



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LA57 UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reserved			
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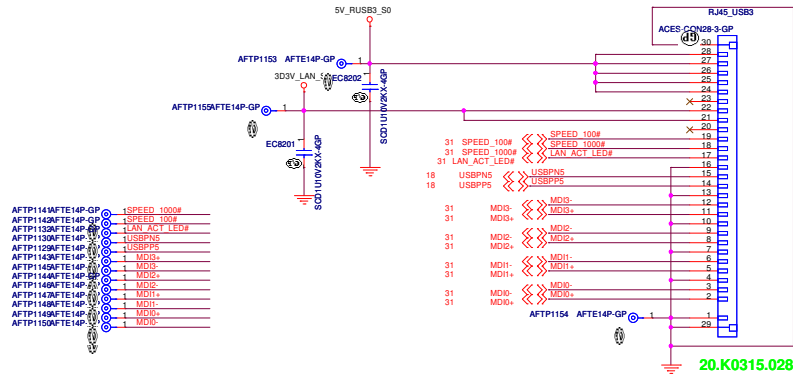
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LA57 UMA

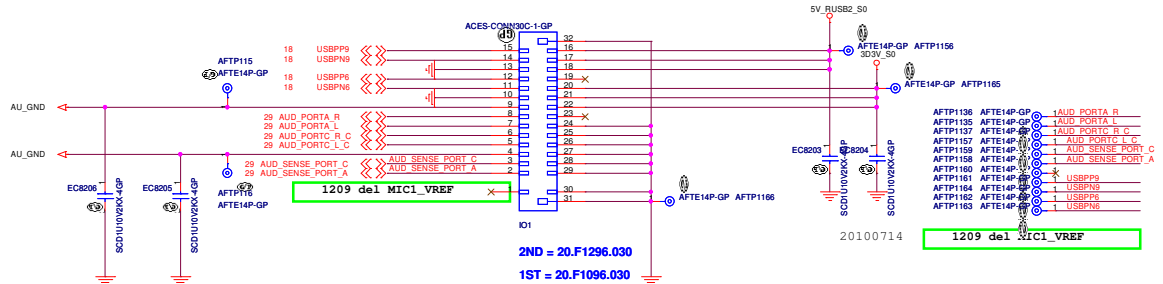
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Title			
Reserved			
Size	Document Number		Rev
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20100728 swap net

RJ45_USB CONN.



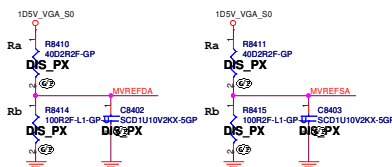
Card Reader Board CONN.



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
IO BD CONN B575	
File	Rev
Size	SA
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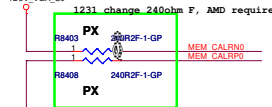
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

1231 change 240ohm F, AMD require

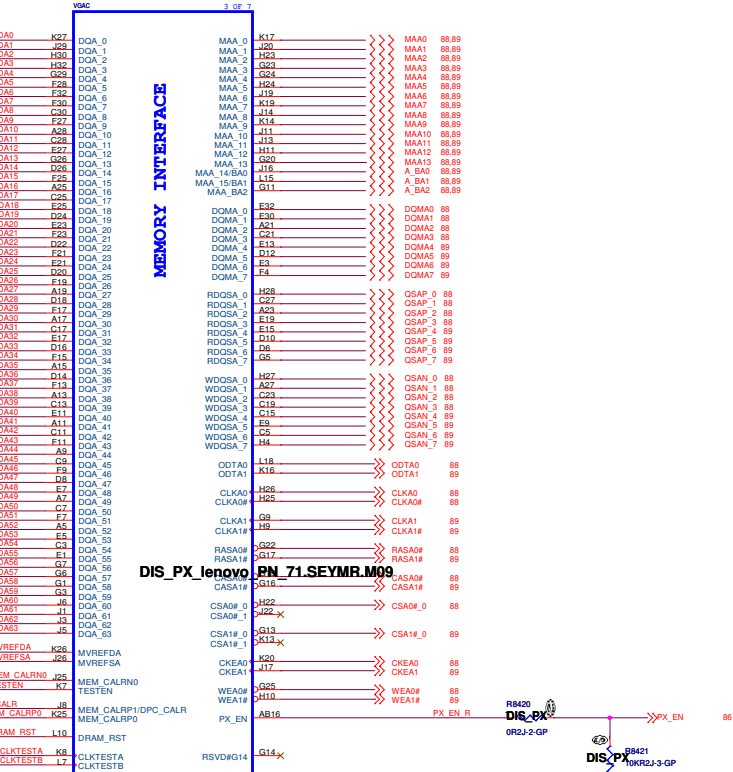


★ This basic topology should be used for DRAM_RST for GDDR3/GDDR5/DDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM Load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

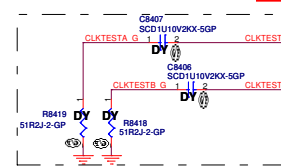
Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except R_MEM_2

DIS_PX lenovo PN 71.SEYMR.M09



71.ROBSON.M12 Colay with Seymour-XT-S3 (71.SEYMR.M01)



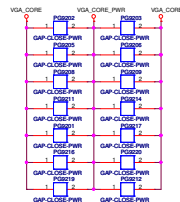
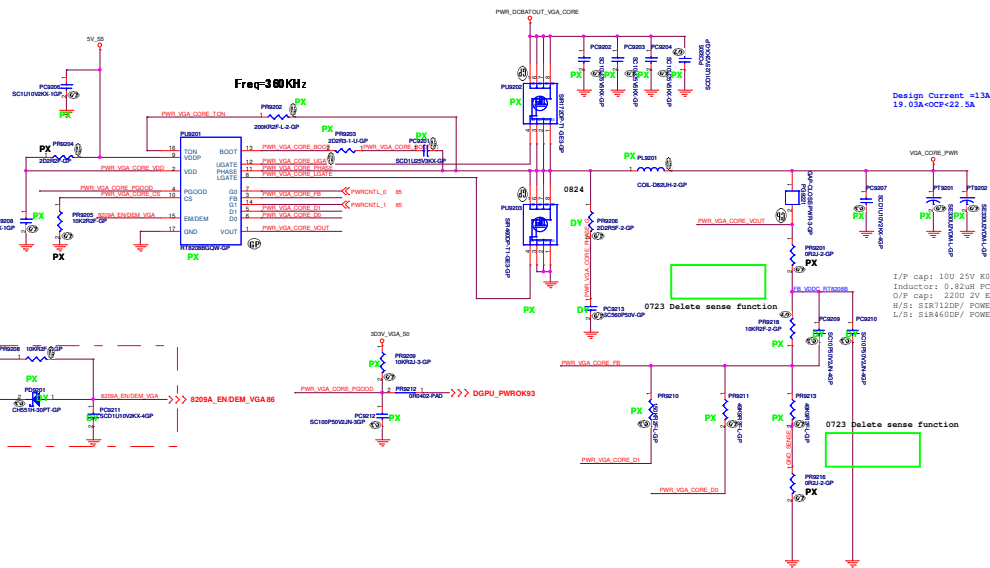
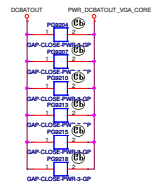
2010/07/06
Schematics check list:
A pull-down resistor is required.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File	GPU Memory(2/5)	Rev	SA
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For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).



Robson-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	L	0.9V
L	L	1.05V
L	L	0.9V

$$V_{out} = 0.75V * (R1 + R2) / R2$$

For ROBSON

PR9210=44K, 2K (64.44225.6DL)

PR9211=150K (64.15035.6DL)

Seymour-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	L	0.9V
L	L	1.05V
H	H	0.9V

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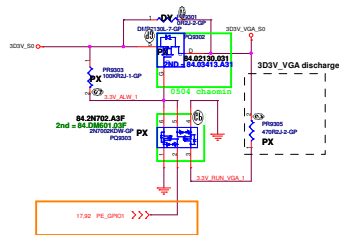
緯創資通 Wistron Corporation

RT8208B +VCC_GFXCORE

B575

Rev 5A

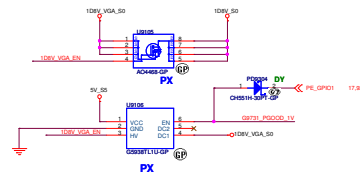
+3VS to 3.3V_DELAY Transfer



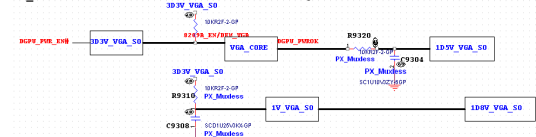
Different To Intel, AMD is High Active

GPU mode	FE_GPI00	FE_GPI01
IGPU	L	R
IGPU with BACO	R	R

G9731 for 1D8V_VGA

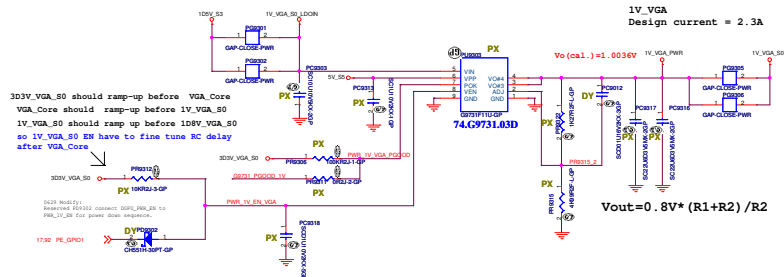


PX_Muxless : value need fine tune for BACO sequence

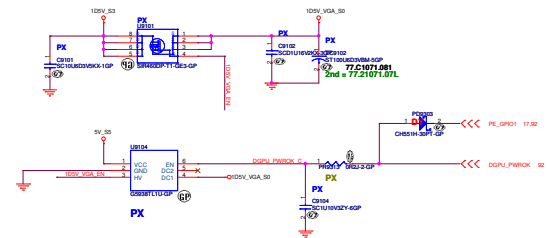


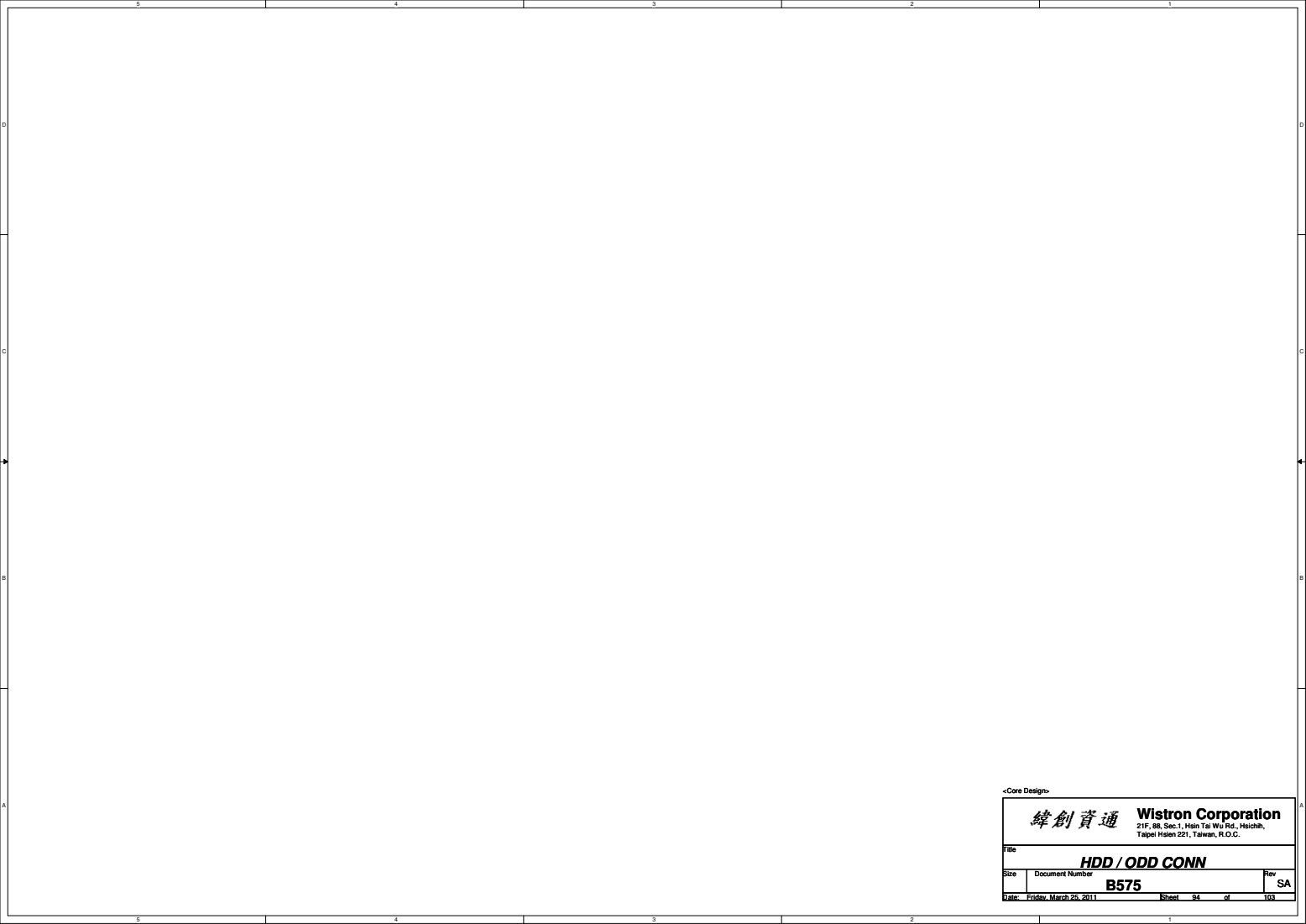
G9731 for 1V_VGA_S0

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whitler_Robson Support BACO, So Change Sequence



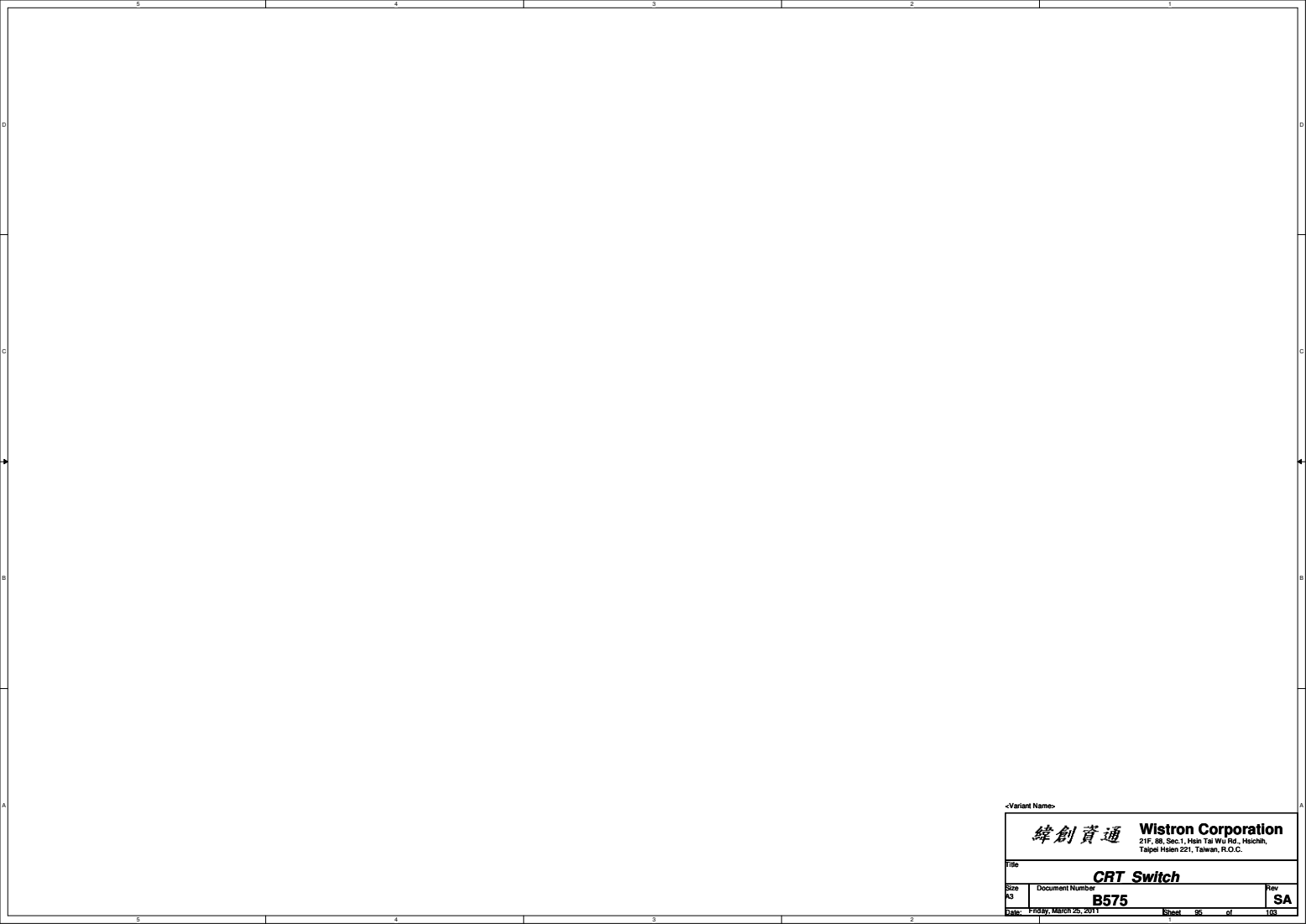
1D5V_VGA_S0





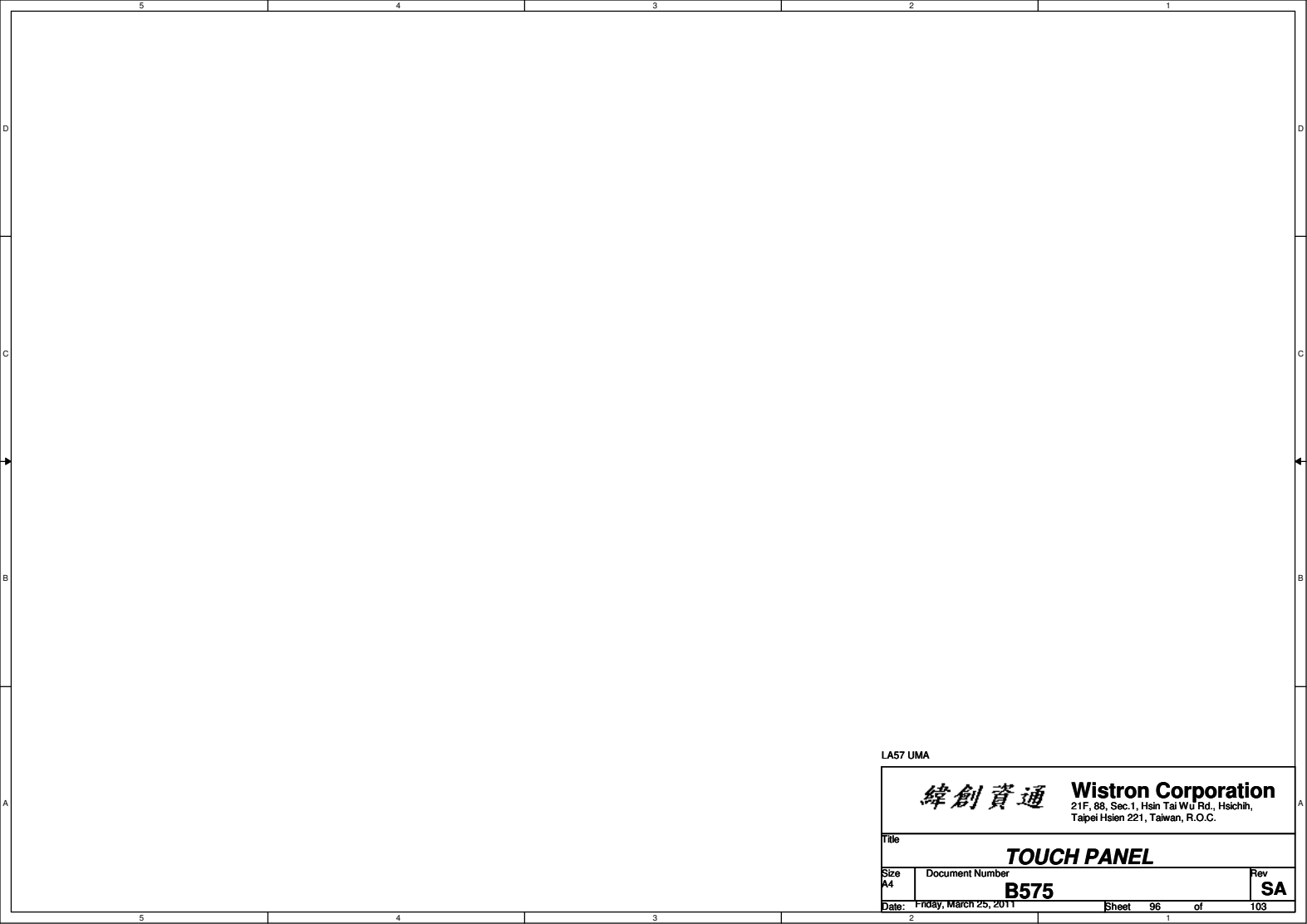
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HDD / ODD CONN			
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	B575		SA
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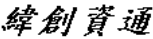


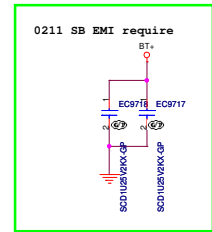
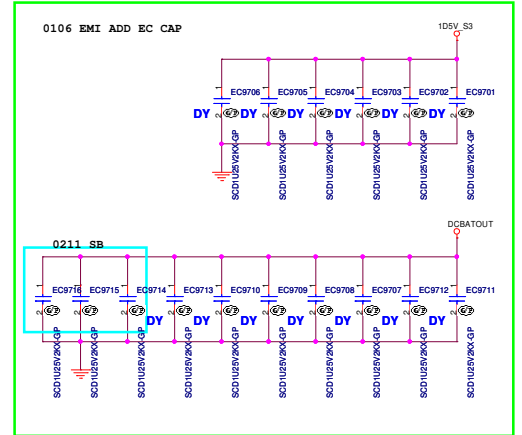
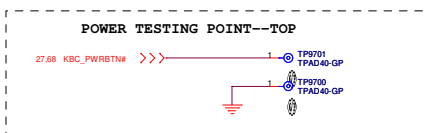
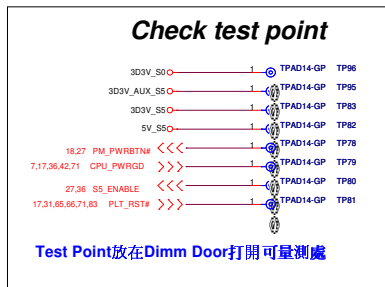
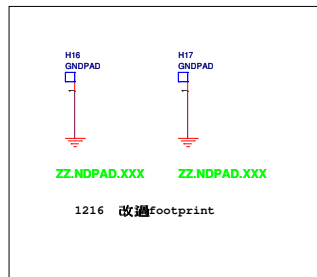
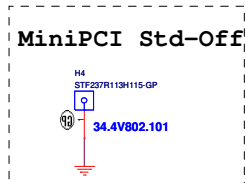
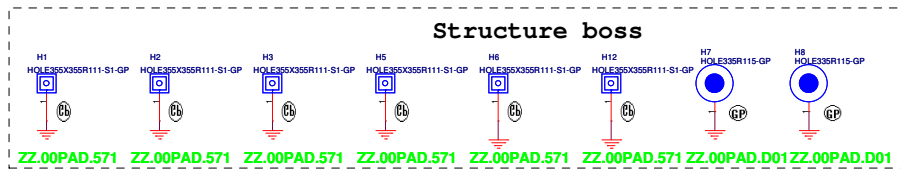
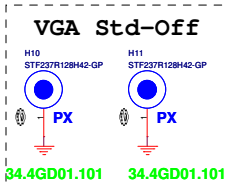
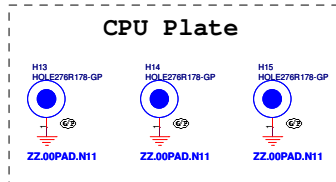
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CRT Switch			
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LA57 UMA

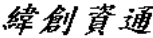
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Title			
TOUCH PANEL			
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Power Delivery Block Diagram

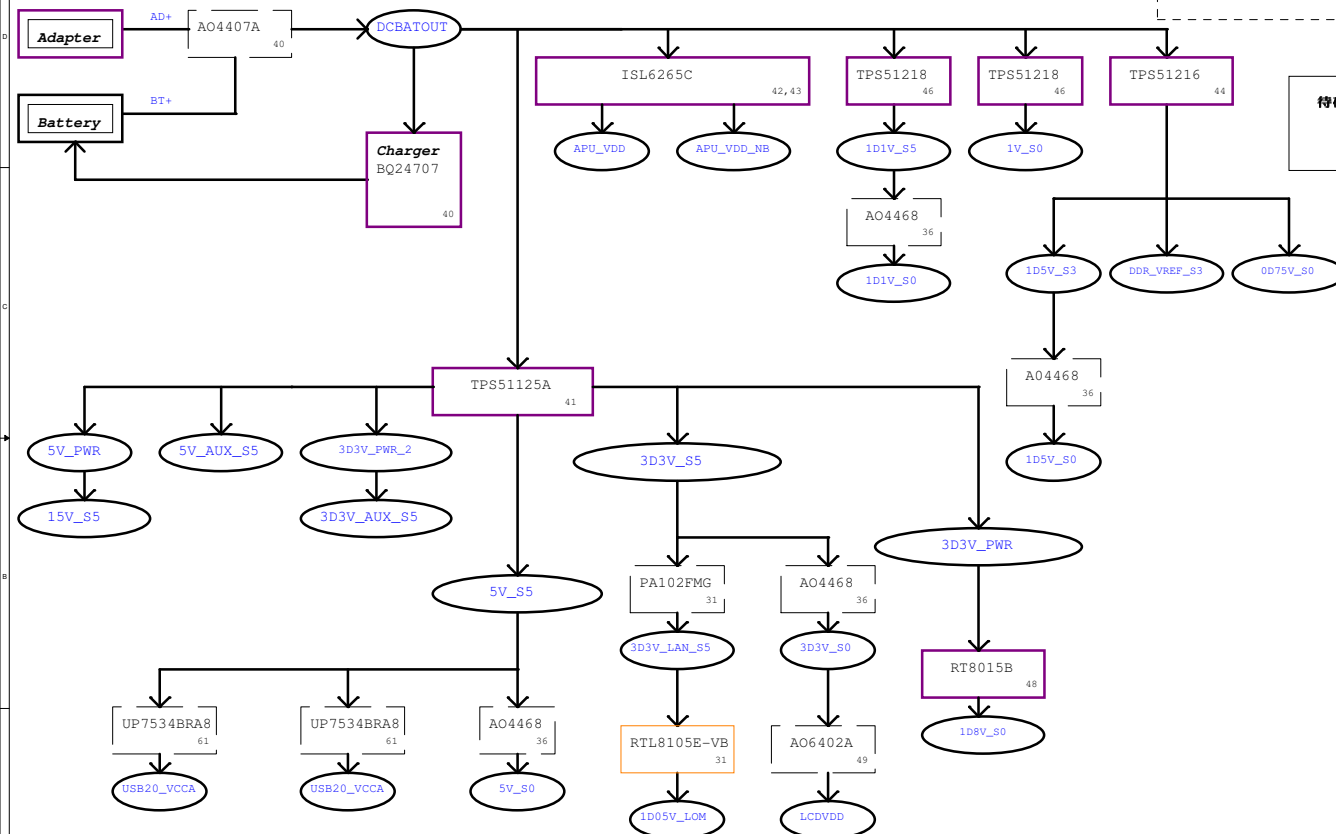
Power Shape

Regulator

LDO

Switch

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Power Block Diagram

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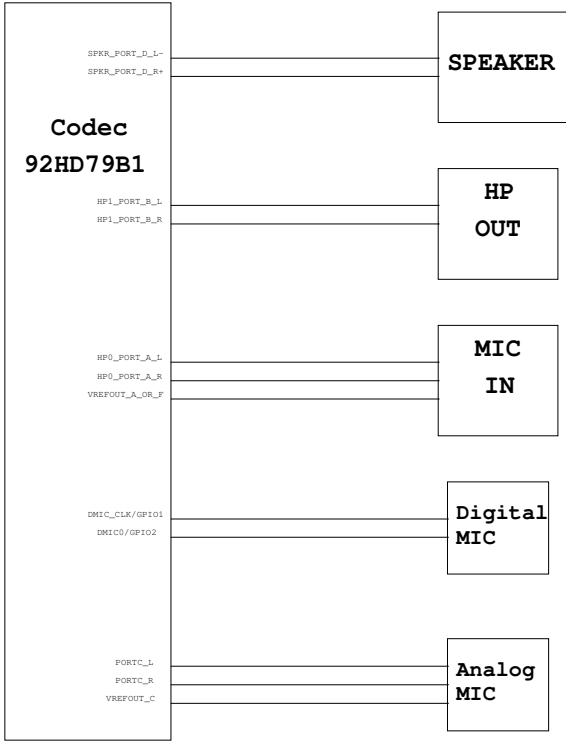
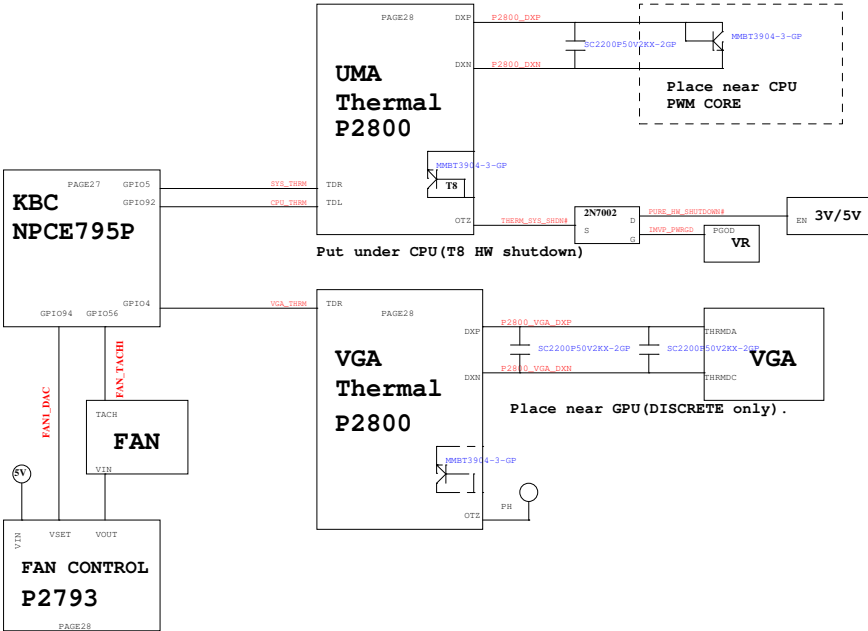
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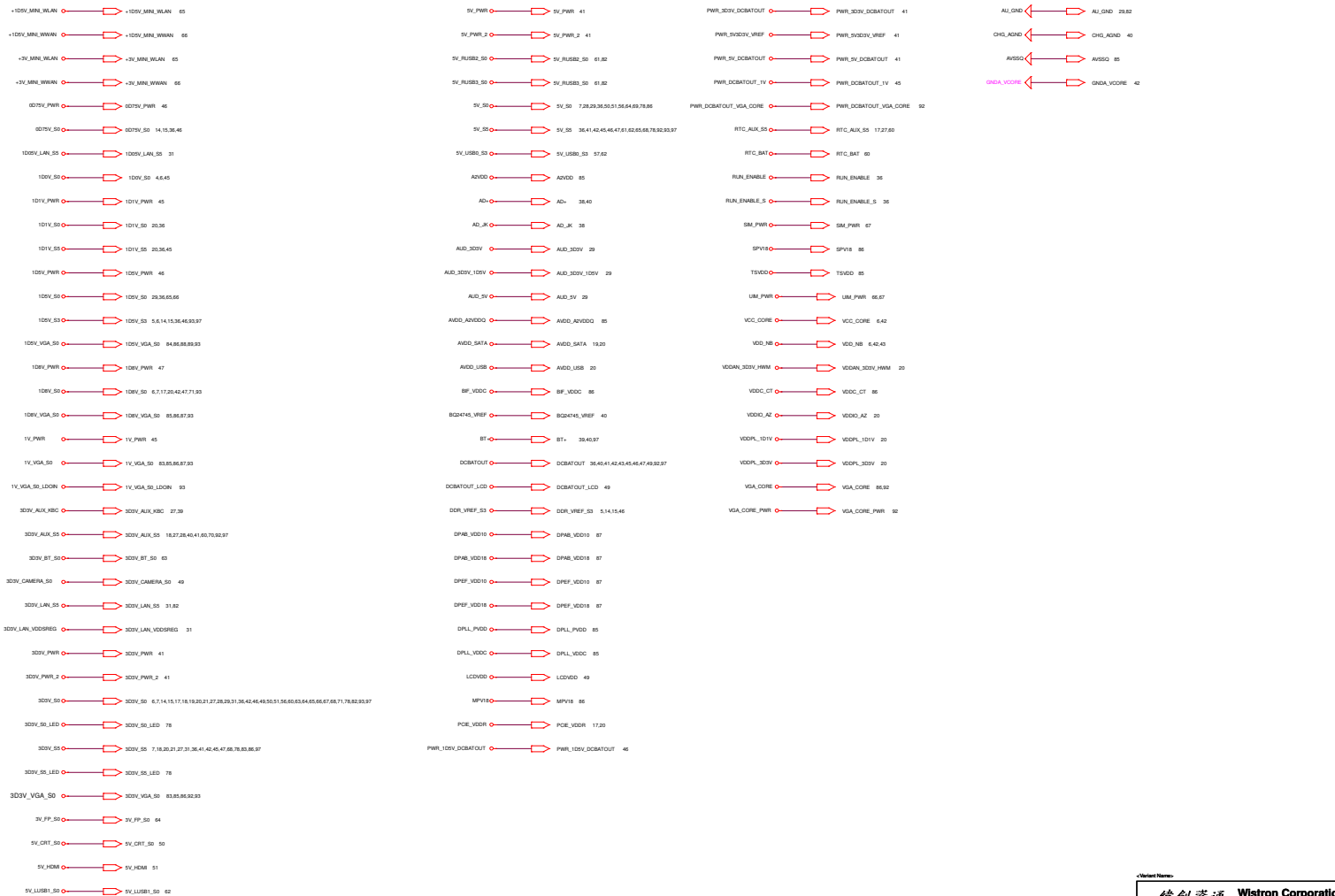
Thermal Block Diagram

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Audio Block Diagram



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